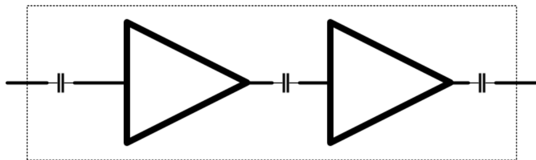
Product Overview

The ASL5006 is a GaN MMIC Low Noise Amplifier (LNA) chip which operates from 5 to 6 GHz. The ASL5006 features extremely flat performance characteristics including 16.5 dB of small signal gain, 2.18 dB of noise figure, output IP3 of +37 dBm and output P1dB of 21.5 dBm across the operating band. With a reflective power limiter, the ASL5006 has a power handling capacity of 37.5 dBm continues wave (CW). Also, ASL5006 can be switched on/off with a digital voltage of 0/3.3 V. This versatile LNA is ideal for hybrid and MCM assemblies due to its compact size, consistent output power and DC blocked RF I/O's. All data is measured with the chip in a 50 Ohm test fixture connected via two 0.025 mm (1 mil) diameter bond wires of minimal length 0.51 mm (20 mil).

Functional Block Diagram



Key Features

1. Integrated DC blocking at RF input/output
2. Enable/Disable mode with digital signal
3. Bandwidth: 5 GHz to 6 GHz
4. Small Signal Gain : 16.5 dB
5. Noise Figure: 2.18 dB
6. Output P1dB: 21.5 dBm
7. Output TOI: 37 dBm
8. Input Power Handling:37.5 dBm(CW), 40.5 dBm (Pulsed)
9. 50 Ohm Matched Input/output
10. Die Size: 3.5 x 1.5 x 0.1 mm

Applications

1. Instrumentation
2. Point-to-point communication

Absolute Maximum Rating

Drain Bias Voltage (VDD)	+40 Vdc
Gate Bias Voltage (VSS)	-10 Vdc
RF Input Power (CW)	37.5 dBm
RF Input Power (Pulsed)	40.5 dBm
Channel Temperature	200 °C
Continuous Pdiss(T = 85 °C)	1.5 W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +65 °C

ELECTROSTATIC SENSITIVE DEVICE OBSERVE HANDLING PRECAUTIONS

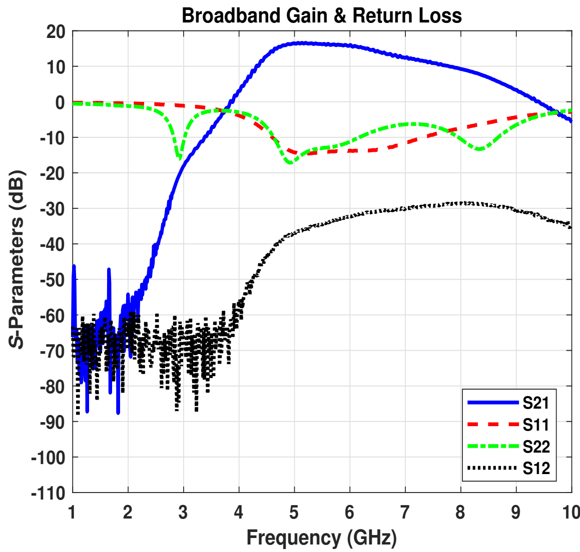
Electrical Specifications

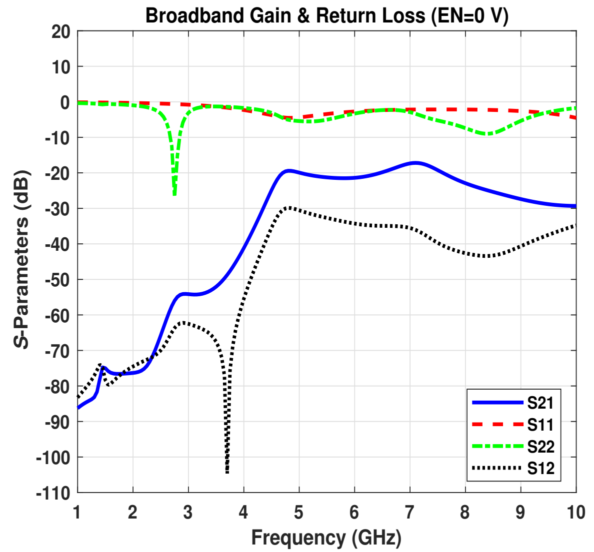
Parameter	Min.	Typ.	Max.	Units
Frequency Range	5	-	6	GHz
Gain	15.8	16	16.5	dB
Noise Figure	2.18	2.3	2.58	dB
Input Return Loss	-	14	-	dB
Output Return Loss	-	13	-	dB
Output Power for 1 dB Compression (P1dB)	-	21.5	-	dBm
Saturated Output Power	-	23.8	-	dBm
Output Third Order Intercept Point (IP3)	-	37	-	dBm
Supply Current (with RF)	-	85	-	mA

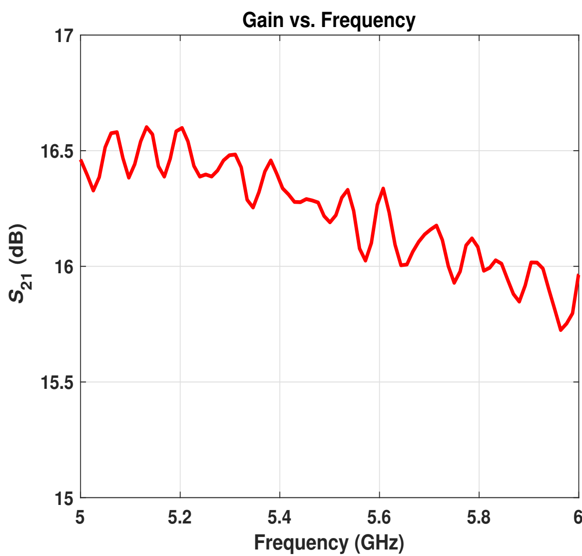
Test conditions unless otherwise noted: TA=+25° C, VDD=10 V, VSS=-6 V, EN=3.3 V, ID=85 mA, Z0=50 Ω
Tcase is Cold Plate temperature, and Base Plate temperature (TBP) is 85°C.

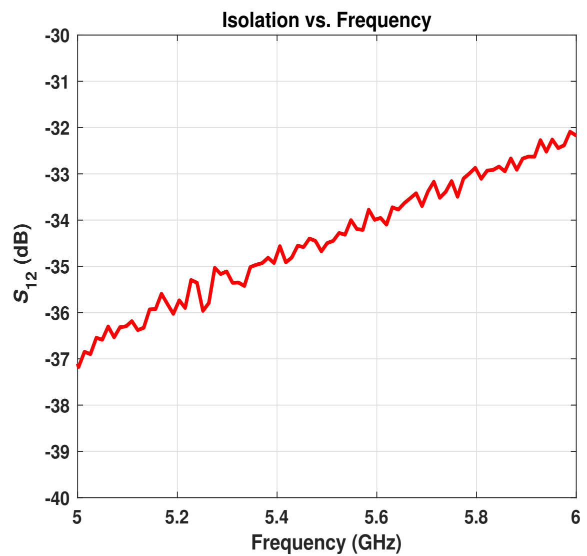
Typical Performance Curves

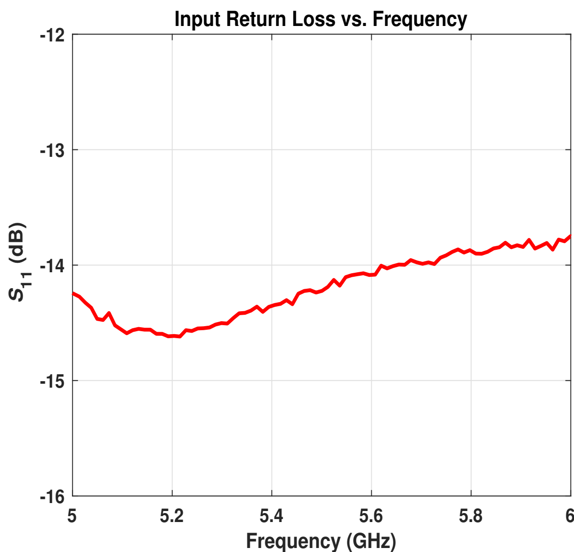
Test conditions unless otherwise noted:VDD=10 V, VSS=-6 V, EN=3.3 V

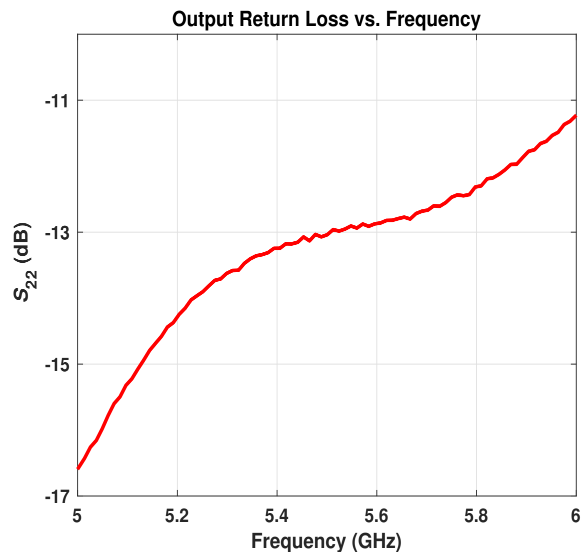






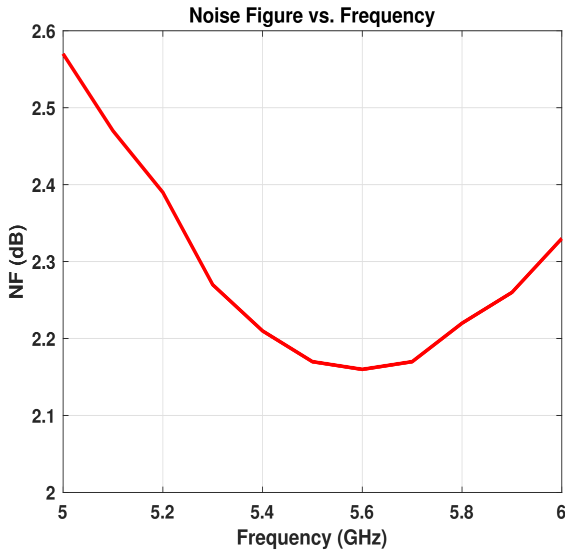


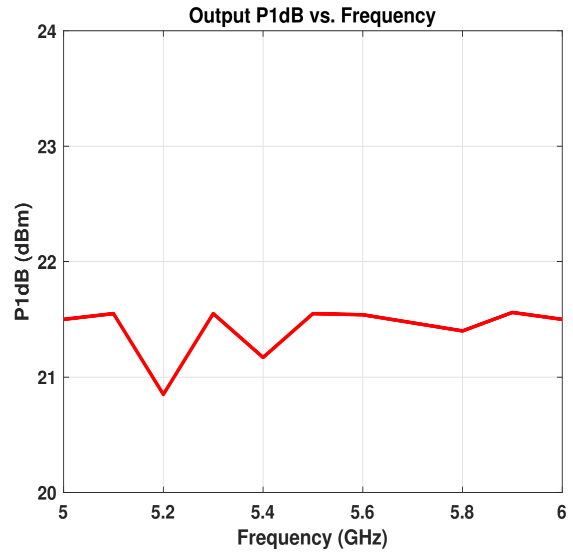


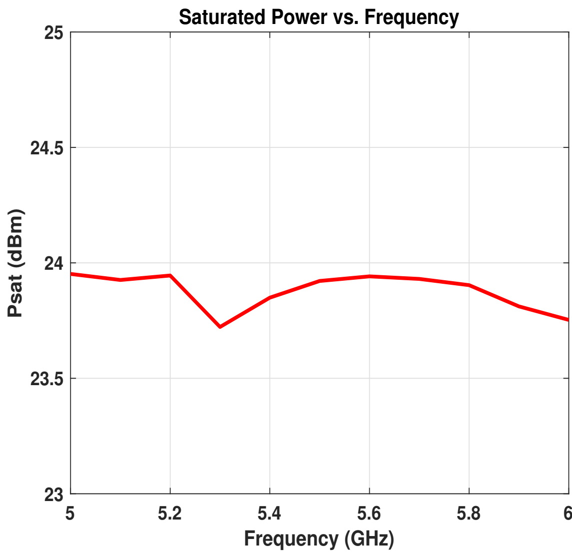


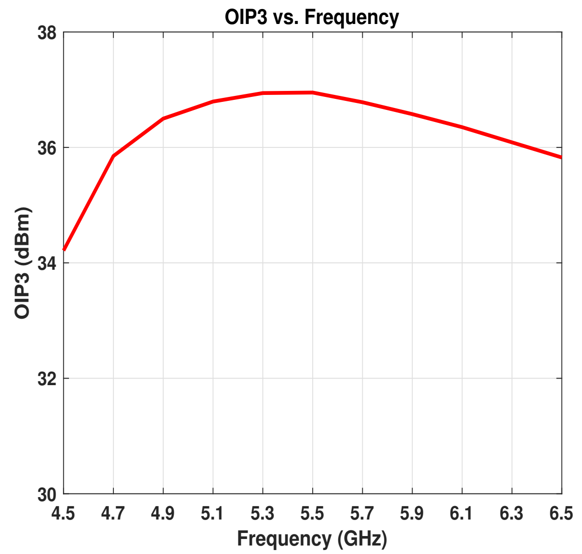
Typical Performance Curves

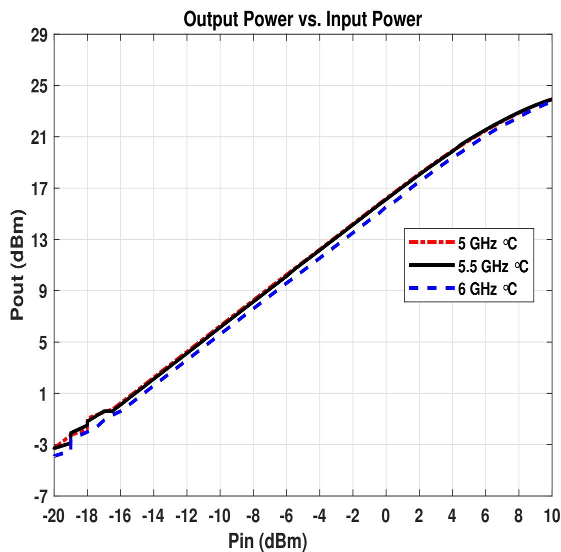
Test conditions unless otherwise noted:VDD=10 V, VSS=-6 V, EN=3.3 V

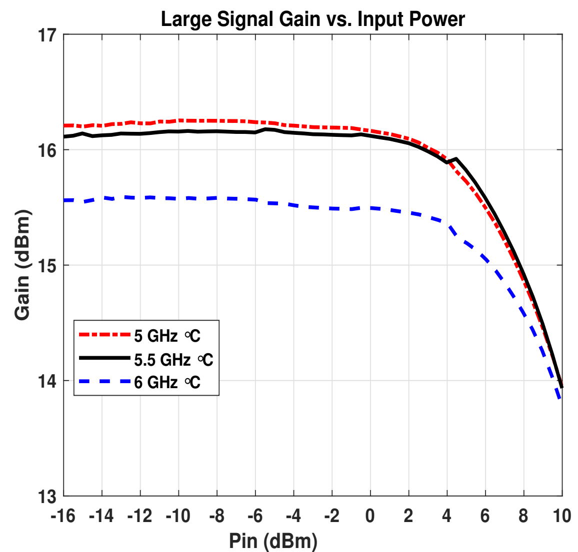




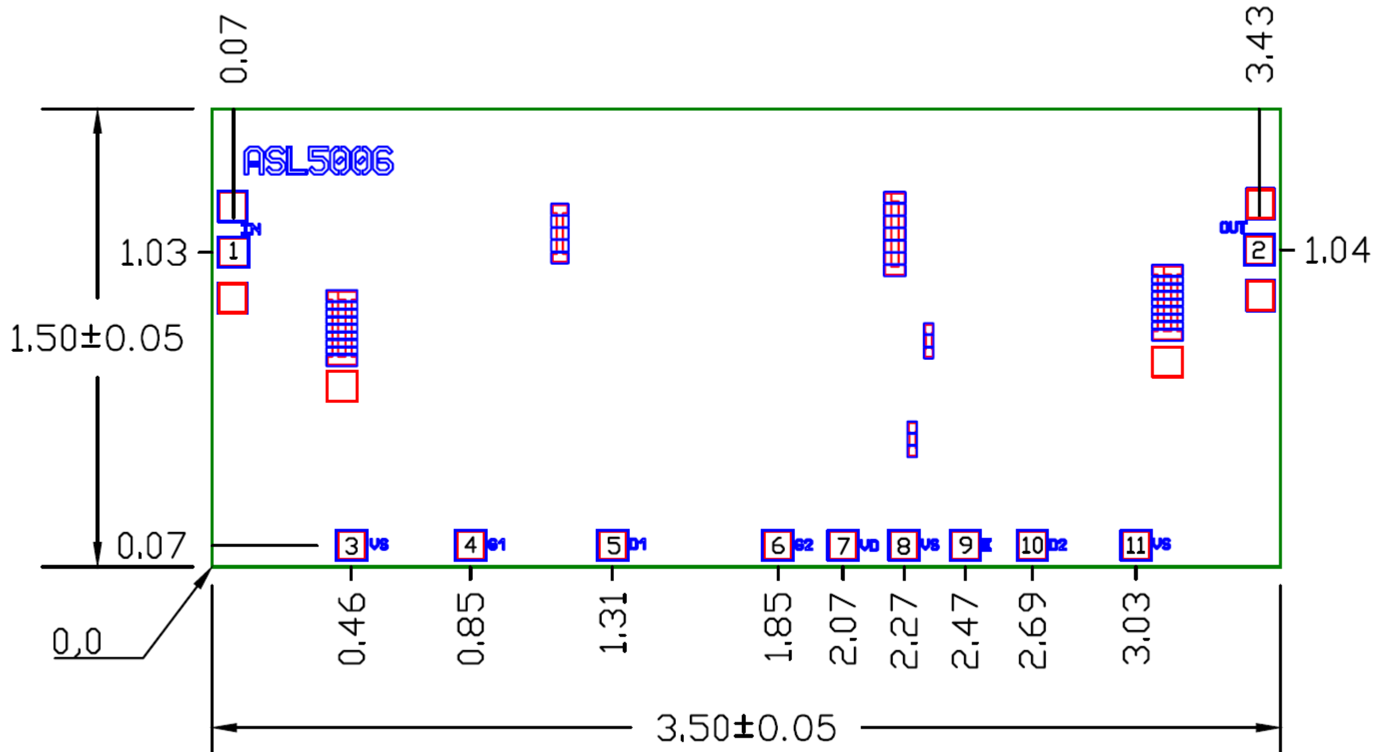








Mechanical Information



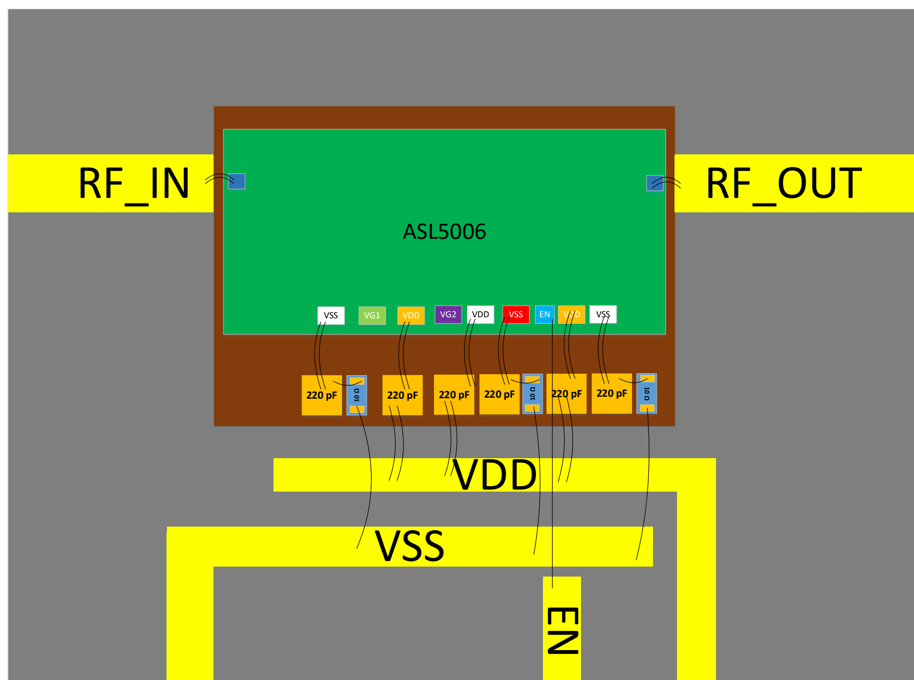
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. CHIP SIZE = 3.5 mm × 1.5 mm (DICING STREET INCLUDED) ± 0.05 mm
3. RF pads (1,2) = 0.1 × 0.1 mm
4. DC pads (3,4,5,6,7,8,9,10,11) = 0.1 × 0.1 mm
5. BACKSIDE METALLIZATION: GOLD
6. BACKSIDE METAL IS GROUND
7. BOND PAD METALIZATION: GOLD
8. NO CONNECTION REQUIRED FOR UNLABELED BOND PADS
9. OVERALL DIE SIZE ±50 µm

Bond Pad Description

1	RF-IN	This pad is AC coupled and matched to 50 Ohms.
2	RF-OUT	This pad is AC coupled and matched to 50 Ohms.
3,11	VSS	Negative Supply Voltage for the amplifier.
4,6	-	Not Connected.
5,10	VDD	Positive Supply Voltage for the amplifier. External bypass capacitors of 220 pF or 150 pF are required.
7	VDD	Positive Supply Voltage for the amplifier. External bypass capacitors of 220 pF or 150 pF are required.
8	VSS	Negative Supply Voltage for the amplifier.
9	EN	This pad is for enabling/disabling of amplifier. A digital signal 0/3.3V. This pad is pulled down internally.

Assembly Diagram



Assembly Notes

Component Placement and Adhesive Attachment Assembly Notes:

1. Use vacuum collet to pick up the die.
2. The force should be controlled during placement and mounting specially no force should be applied to air bridges.

Reflow process assembly notes:

1. Use CMC or MoCu carrier to decrease thermal expansion mechanical stress
2. Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3-4 minutes, maximum.
3. An alloy station or conveyor furnace with reducing atmosphere should be used.
4. Do not use any kind of flux.
5. Devices must be stored in a dry nitrogen atmosphere.
6. Use Au bond wire.

Contact Information

For the latest specifications, additional product information:
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