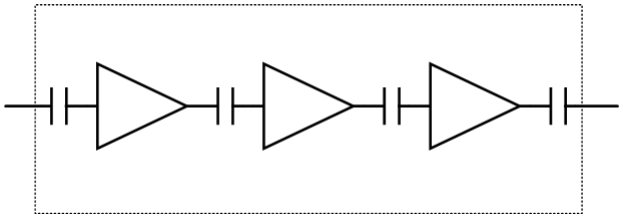
Product Overview

The ASA6018 is a GaN MMIC three-stage power amplifier designed for X-band applications. The amplifier provides 26.2 dB of power gain, +34.2 dBm of saturated power and 43% PAE from a +16V supply voltage. All data is measured with the chip in a 50 Ohm test fixture connected via two 0.025 mm (1 mil) diameter bondwires of minimal length 0.51 mm (20 mil).

Key Features

1. Integrated DC blocking at RF input/output
2. Frequency Range: 8.5 GHz to 10.5 GHz
3. Power Gain: 26.2 dB
4. PAE: 43%
5. Saturated Output Power: +34.2 dBm
6. 50 Ohm Matched Input/output
7. Die Size: 3.5 x 1.16 x 0.1 mm

Functional Block Diagram



•VGT1 to drive first stage in class AB.

Applications

1. General Communication Applications
2. VSAT
3. Point to Point Radios

Absolute Maximum Rating

Drain Bias Voltage (VDD)	+40 Vdc
Gate Bias Voltage (VGG)	-8 Vdc
Drain Current (ID)	0.5 A
RF Input Power (Pin),CW,50 Ω,(VDD = +25 V)	14 dBm
Channel Temperature	200 °C
Continuous Pdiss(T = 85 °C)	6 W
Storage Temperature	-65 to +150 °C

Typical Supply Current vs. VDD

Parameter	Value/Range
VDD	16 V
ID @ VGG=-4 V	280 mA with RF, 0 mA without RF
Operating Temperature	-40 to +85 °C

1. Currents are measured at 15 °C.
2. The typical operation of amplifier is for supply voltages VGG =-3.4 V and VDD =+16 V.


ELECTROSTATIC SENSITIVE DEVICE OBSERVE HANDLING PRECAUTIONS

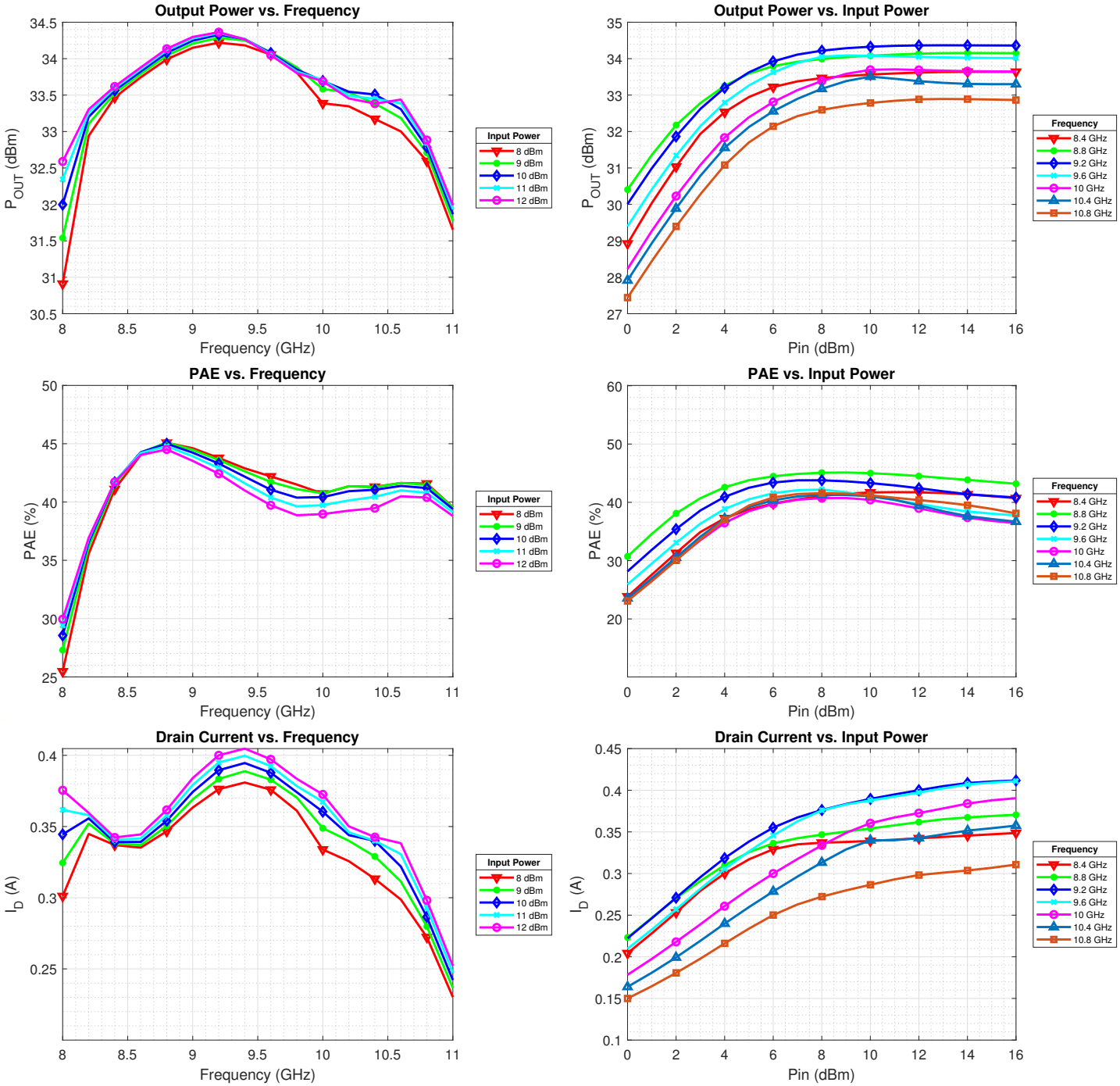
Electrical Specifications

Parameter	Min.	Typ.	Max.	Units
Frequency Range	-	8.5-10.5	-	GHz
Power Gain	25	25.5	26.2	dB
Small Signal Gain (IDQ = 70 mA)	28	30	30	dB
Input Return Loss	-	15	-	dB
Power Added Efficiency (PAE)	42	42.3	43	%
Saturated Output Power	33	33.5	34.2	dBm
Supply Current (with RF)	320	330	380	mA

Test conditions unless otherwise noted: Tcase=15 °C, VDD=16 V, VGG=-3.4 V, IDQ=0 mA, Z0=50 Ω, Pin=8 dBm
Tcase is Cold Plate temperature, and Base Plate temperature (TBP) is 85°C.

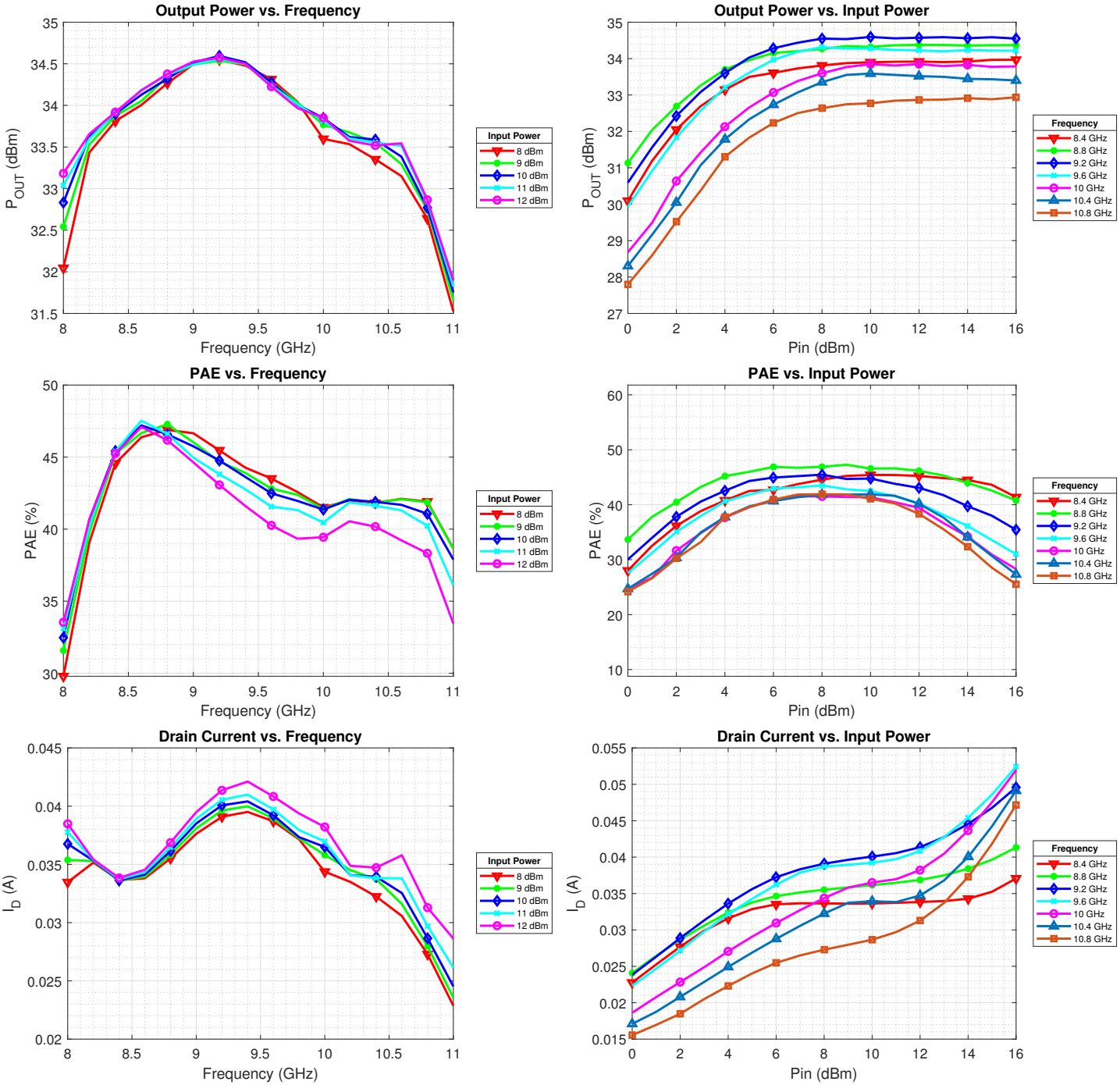
Performance Plots – Large Signal

Test conditions unless otherwise noted:VDD=16 V, VGG=-3.4 V, Tcase=15 °C, CW, Class AB (VGT1 Applied)



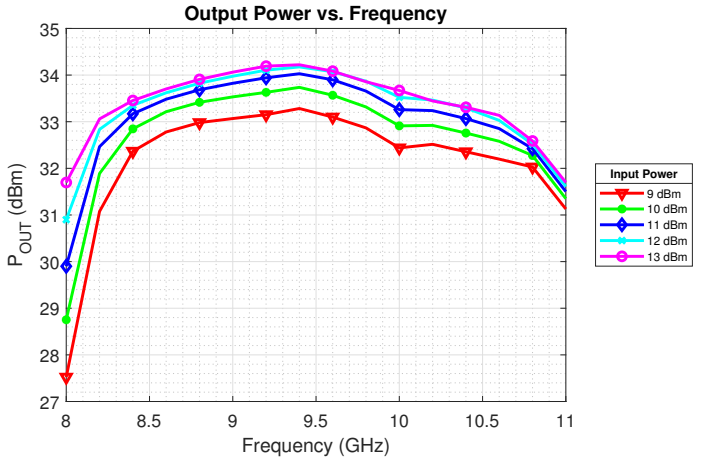
Performance Plots – Large Signal

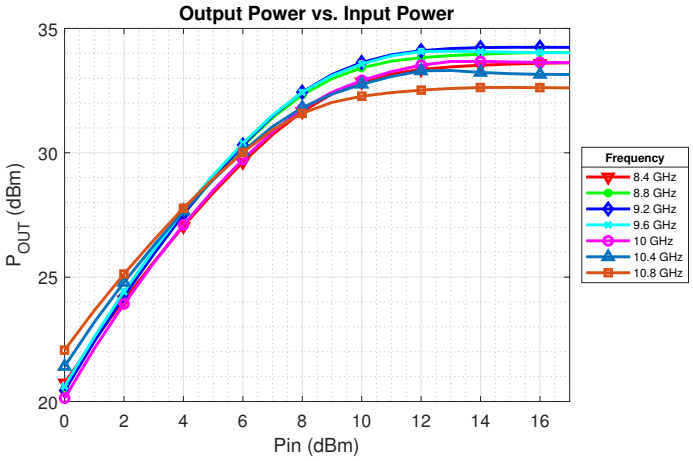
Test conditions unless otherwise noted:VDD=16 V, VGG=-3.4 V, Tcase=15 °C, 1 KHz Pulse 10%, Class AB (VGT1 Applied)

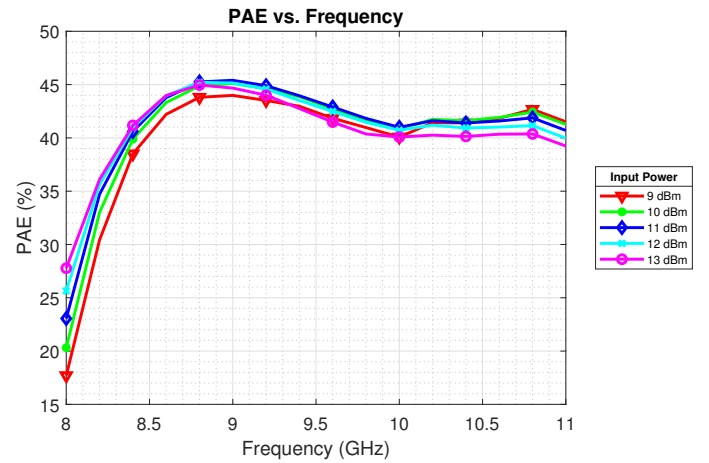


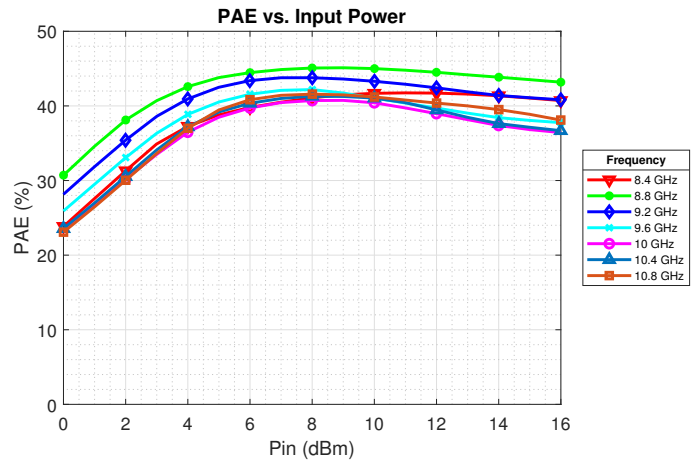
Performance Plots – Large Signal

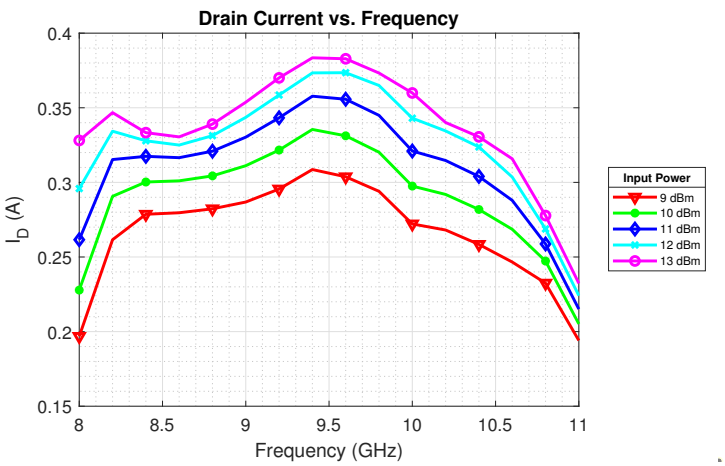
Test conditions unless otherwise noted:VDD=16 V, VGG=-3.4 V, Tcase=15 °C, CW, Class C (VG1 Applied)

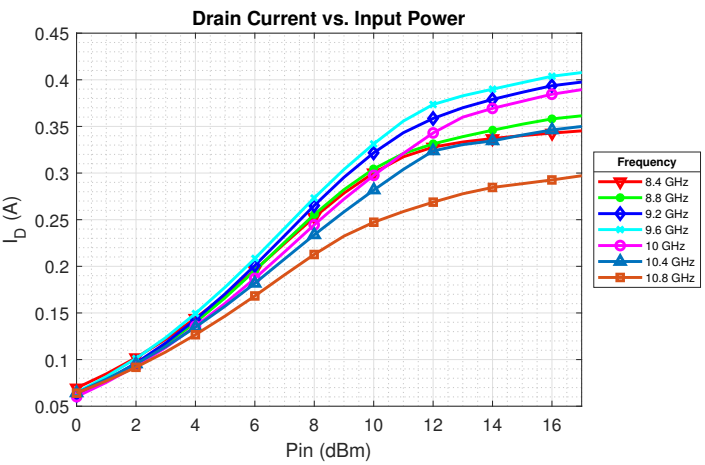






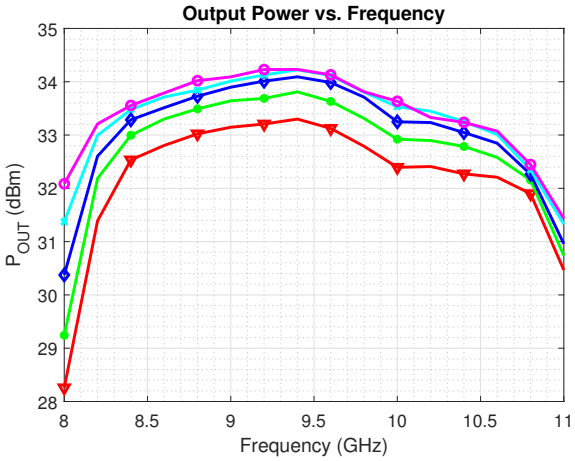


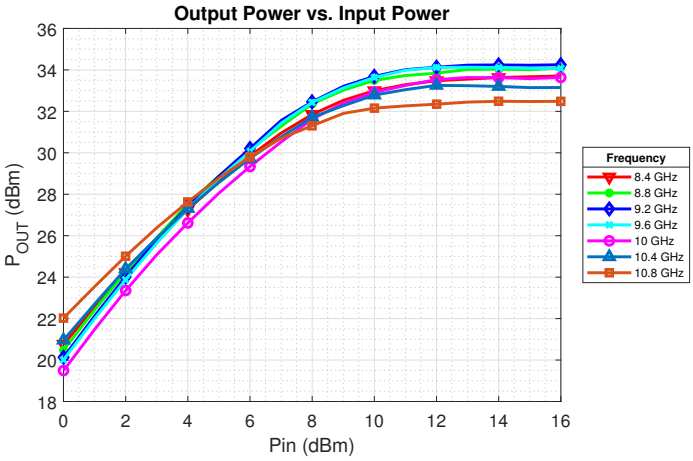


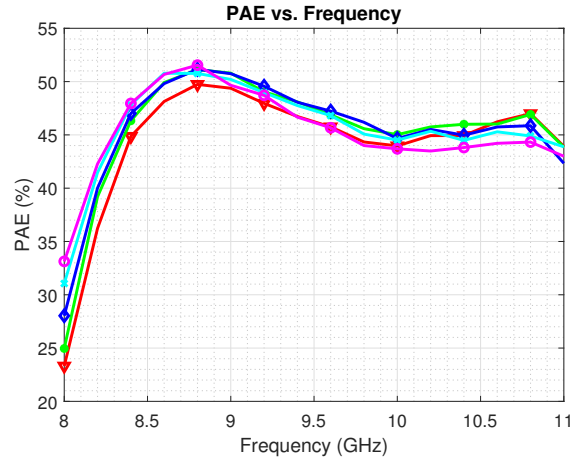


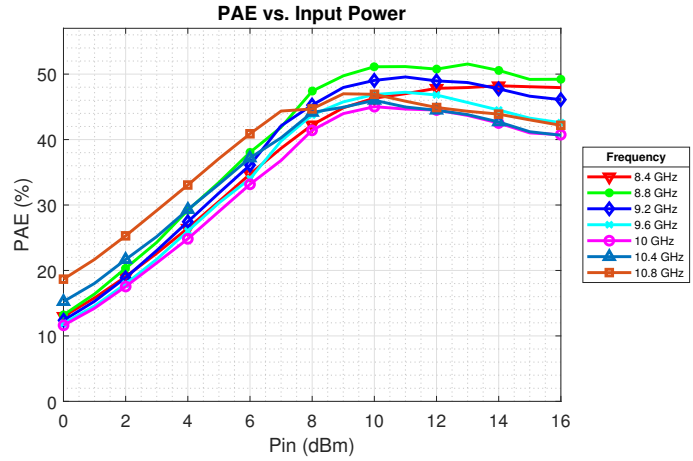
Performance Plots – Large Signal

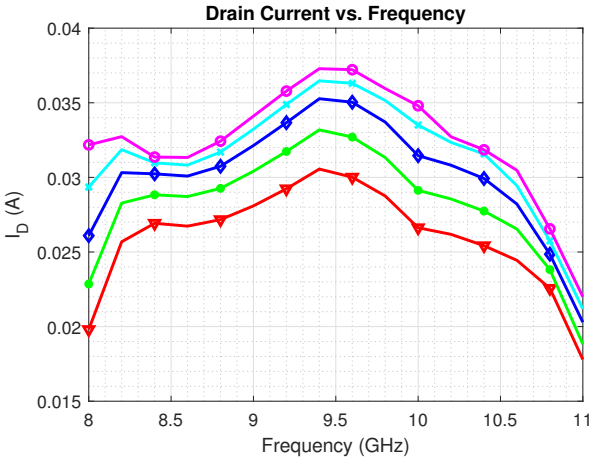
Test conditions unless otherwise noted:VDD=16 V, VGG=-3.4 V, Tcase=15 °C, 1 KHz Pulse 10%, Class C (VG1 Applied)

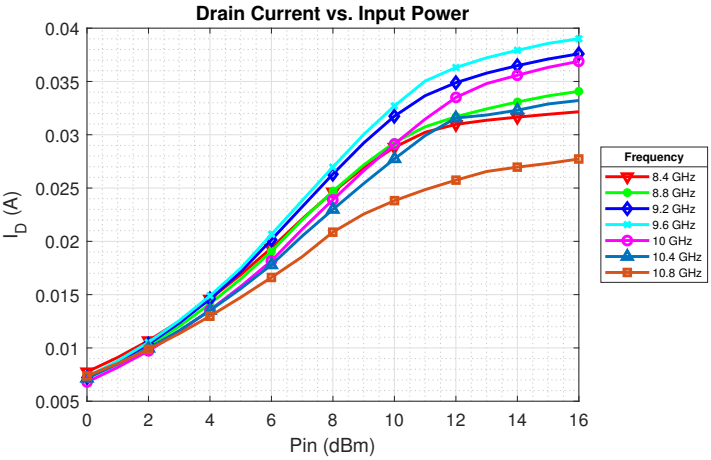






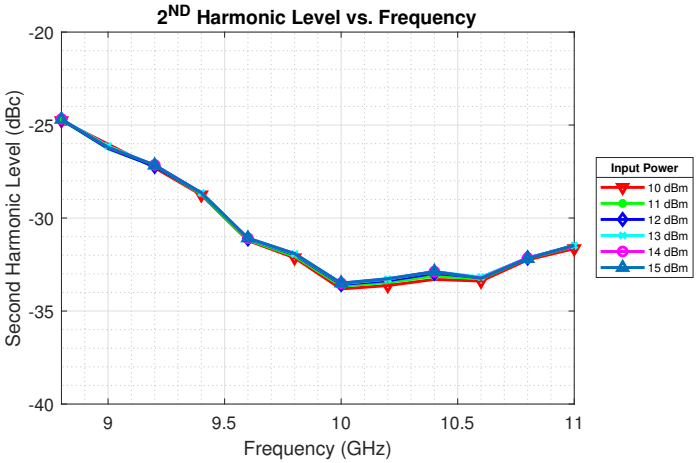


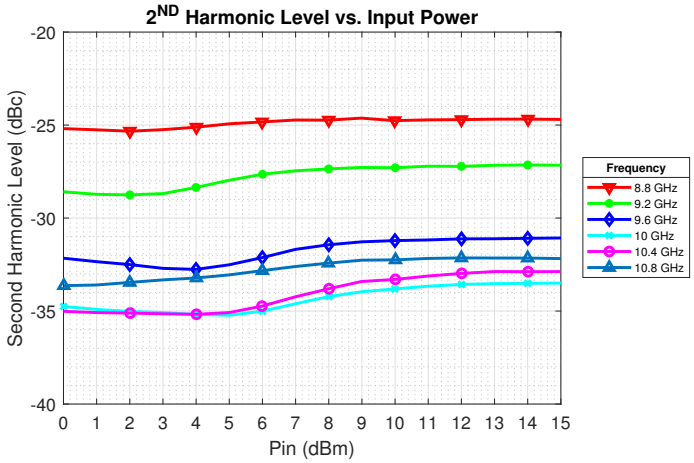




Performance Plots – Linearity

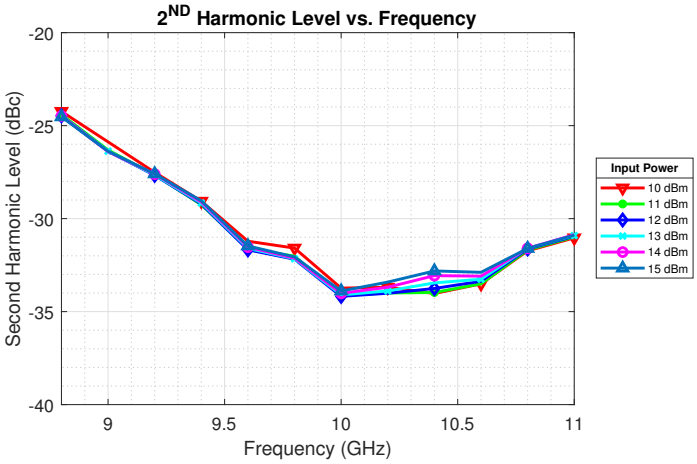
Test conditions unless otherwise noted:VDD=16 V, VGG=-3.4 V, Tcase=15 °C, Class AB (VGT1 Applied)

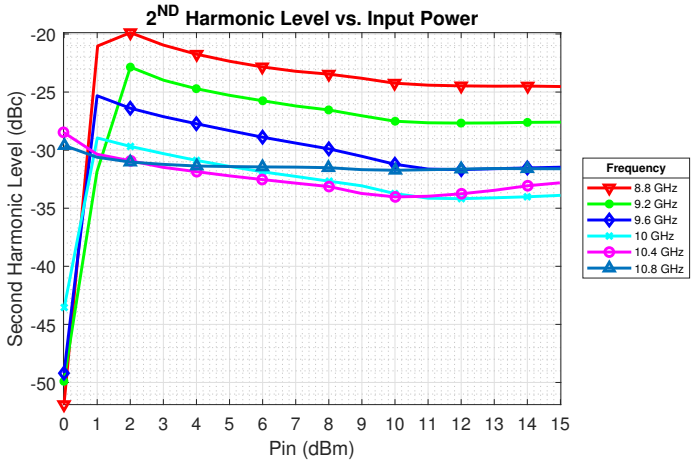




Performance Plots – Linearity

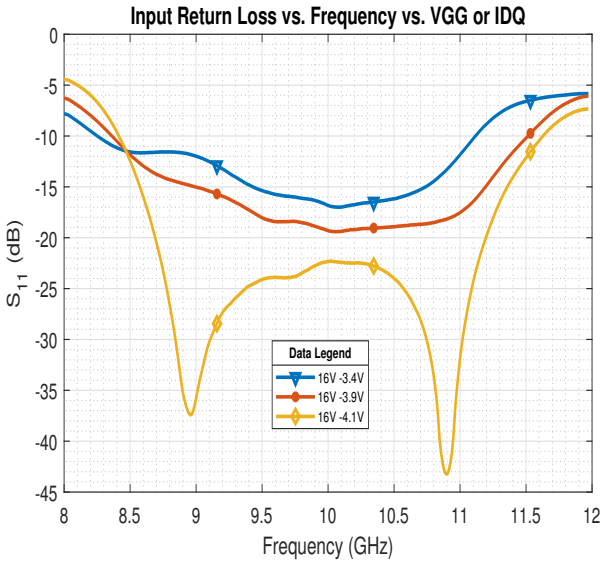
Test conditions unless otherwise noted:VDD=16 V, VGG=-3.4 V, Tcase=15 °C, Class C (VG1 Applied)

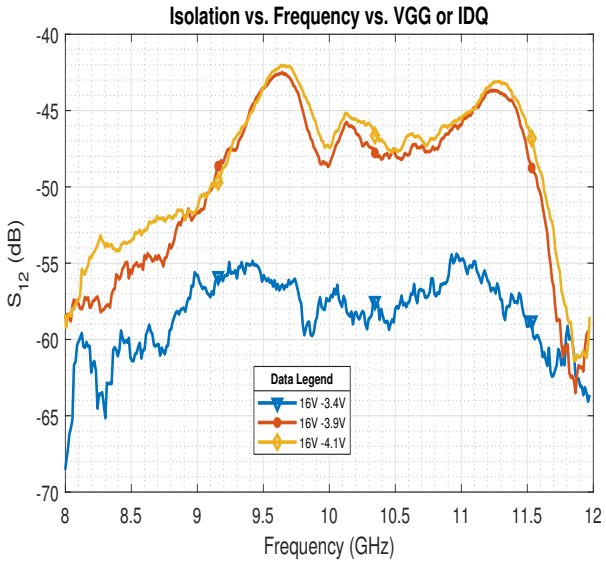


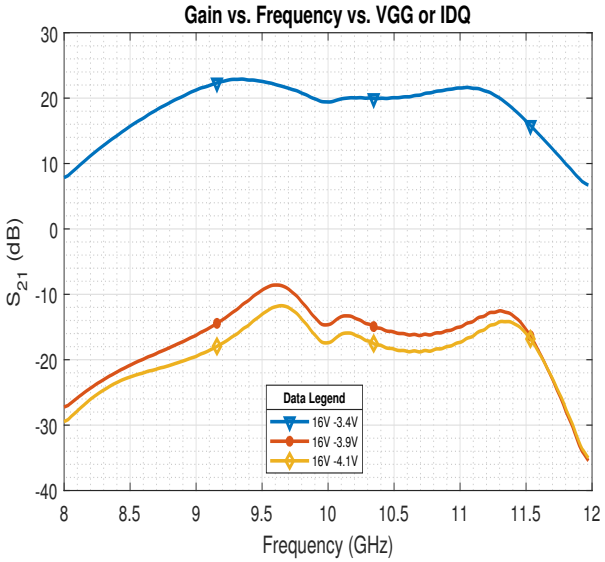


Performance Plots – Small Signal (VGT1 Applied)

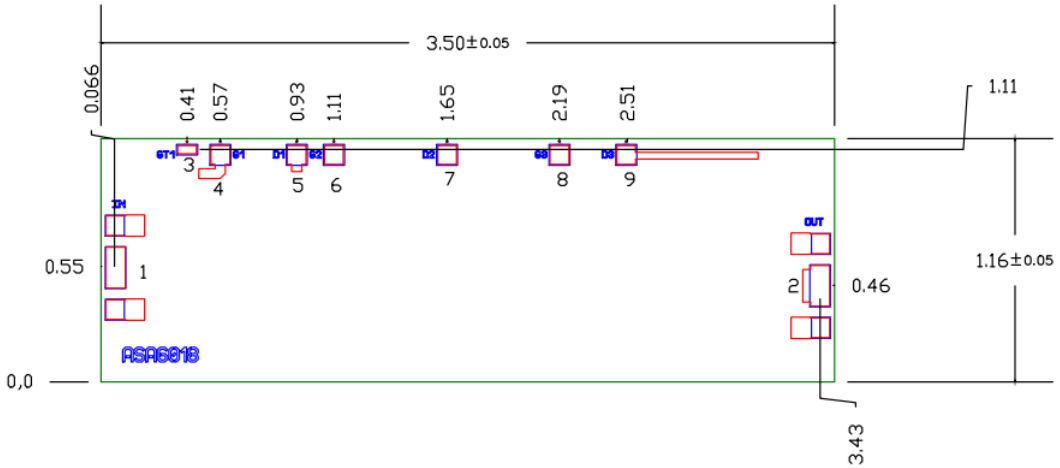
Test conditions unless otherwise noted:VDD=16 V, Tcase=15 °C, ID= 70 mA







Mechanical Information



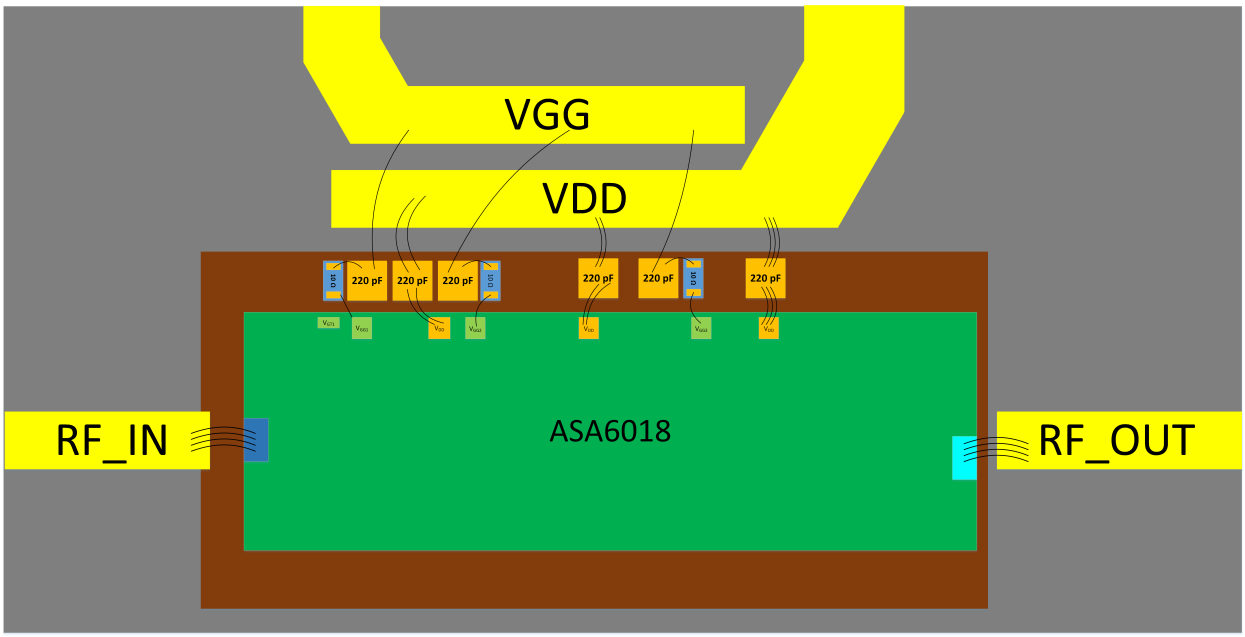
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. CHIP SIZE = 3.5 mm × 1.16 mm (DICING STREET INCLUDED) ± 0.05 mm
3. RF pads (1,2) = 0.1 × 0.15 mm
4. DC pads (3) = 0.1 × 0.1 mm
5. DC pads (4,5,6,7,8,9) = 0.06 × 0.07 mm
6. BACKSIDE METALLIZATION: GOLD
7. BACKSIDE METAL IS GROUND
8. BOND PAD METALIZATION: GOLD
9. NO CONNECTION REQUIRED FOR UNLABELED BOND PADS
10. OVERALL DIE SIZE ±50 µm

Bond Pad Description

1	RF-IN	This pad is AC coupled and matched to 50 Ohms.
2	RF-OUT	This pad is AC coupled and matched to 50 Ohms.
3	VGT1	Negative Supply Voltage to drive 1st stage in class AB. Do not connect VGG1, when using VGT1.
5,7,9	VDD	Positive Supply Voltage for the amplifier. External bypass capacitors of 220 pF are required.
4	VGG1	Negative Supply Voltage for the amplifier. Do not connect VGT1, when using VGG1.
6	VGG2	Negative Supply Voltage for the amplifier.
8	VGG3	Negative Supply Voltage for the amplifier.

Assembly Diagram



Assembly Notes

Component Placement and Adhesive Attachment Assembly Notes:

1. Use vacuum collet to pick up the die.
2. The force should be controlled during placement and mounting specially no force should be applied to air bridges.

Reflow process assembly notes:

1. Use CMC or MoCu carrier to decrease thermal expansion mechanical stress
2. Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3-4 minutes, maximum.
3. An alloy station or conveyor furnace with reducing atmosphere should be used.
4. Do not use any kind of flux.
5. Devices must be stored in a dry nitrogen atmosphere.
6. Use Au bond wire.

Contact Information

For the latest specifications, additional product information:
Web: www.abba-semi.com
Email: info@abba-semi.com