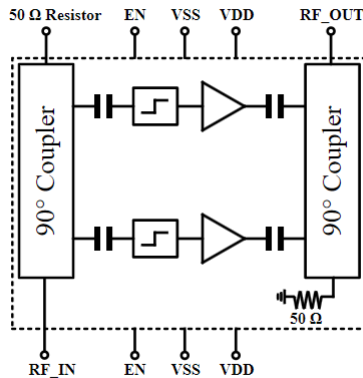


Product Overview

The ASL5003 is a GaAs PHEMT MMIC Low Noise Amplifier (LNA) chip which operates from 4.5 to 7 GHz. The ASL5003 features extremely flat performance characteristics including 15 dB of small signal gain, 2.3 dB of noise figure, output IP3 of +33 dBm and output P1dB of +20 dBm across the operating band. With a reflective power limiter, the ASL5003 has a power handling capacity of 5 W continuous wave (CW) with a fast recovery time of 100 ns. Also, ASL5003 can be switched on/off with a digital voltage of 0/2.5 V. This versatile LNA is ideal for hybrid and MCM assemblies due to its compact size, consistent output power and DC blocked RF I/O's. All data is measured with the chip in a 50 Ohm test fixture connected via two 0.025 mm (1 mil) diameter bondwires of minimal length 0.51 mm (20 mil).

Functional Block Diagram



Key Features

1. Fully integrated, high performance Balanced LNA with built-in limiter
2. Integrated DC blocking at RF input/output
3. Enable/Disable mode with digital signal
4. Bandwidth: 4.5 GHz to 7 GHz
5. Power Gain: 15 dB
6. Low Noise Figure: 2.3 dB
7. High Output IP3: +33 dBm
8. Output P1dB: +20 dBm
9. Gain Flatness: ± 0.1 dB (over 5 to 6 GHz)
10. Power Handling: 5W (CW), 15W (Pulsed)
11. Fast Recovery Time: <100 ns
12. 50 Ohm Matched Input/output
13. Die Size: 2.92 x 3.41 x 0.1 mm

Applications

1. IEEE 802.11a/n/ac Wi-Fi, WLAN
2. Smartphones, tablets, net-books, and other portable computing devices
3. Access points, routers, gateways
4. Wireless video
5. LTE advanced in unlicensed spectrum(LTE-U)
6. General-purpose ISM applications

Absolute Maximum Rating

Drain Bias Voltage (VDD)	+3.5 Vdc
Gate Bias Voltage (VSS)	-3.5 Vdc
RF Input Power (CW)(VDD = +2.5 Vdc)	37 dBm
RF Input Power (Pulsed)(VDD = +2.5 Vdc)	42 dBm
Channel Temperature	175 °C
Continuous P _{diss} (T = 85 °C)	0.55 W
Thermal Resistance (channel to ground pad)	55 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C



ELECTROSTATIC SENSITIVE DEVICE OBSERVE HANDLING PRECAUTIONS

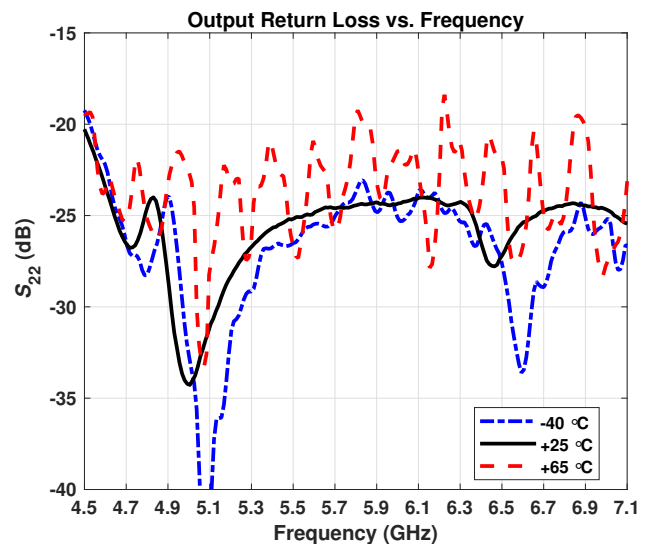
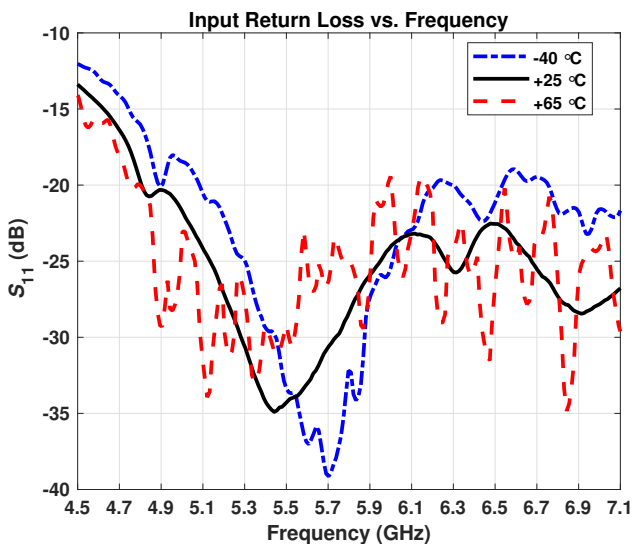
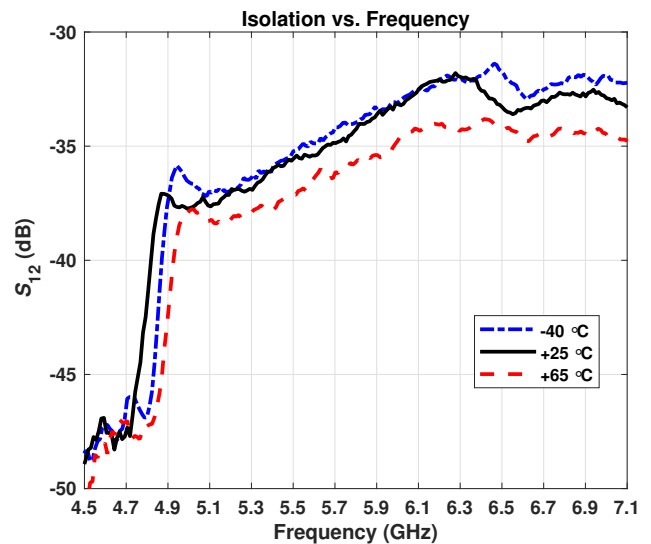
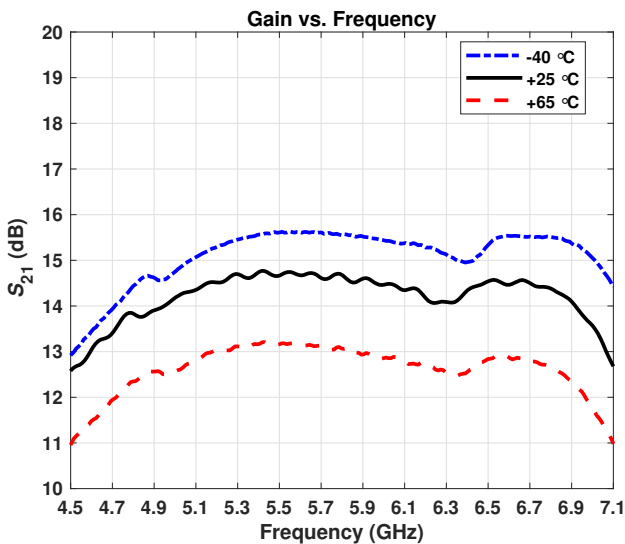
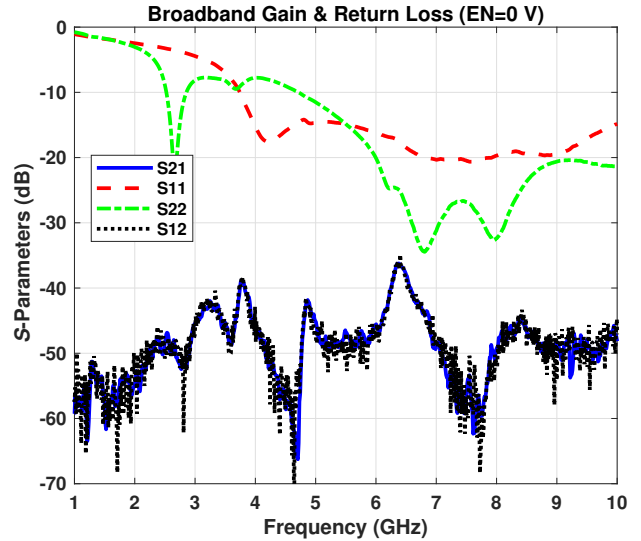
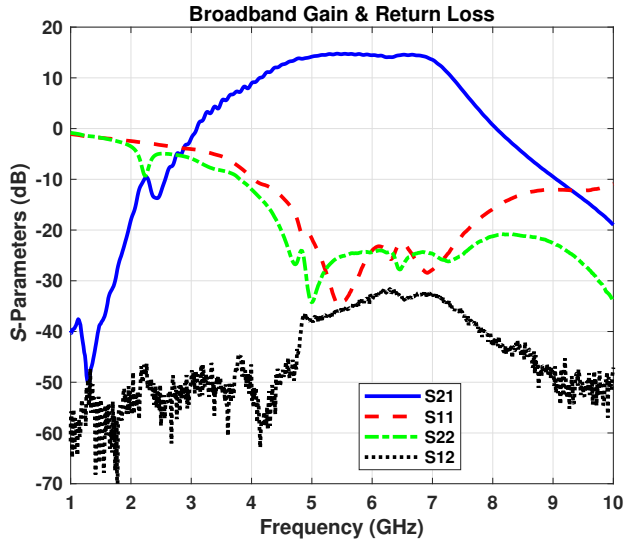
Electrical Specifications

Parameter	Min.	Typ.	Max.	Units
Frequency Range	-	4.5 – 7	-	GHz
Gain	14.5	15	-	dB
Noise Figure	-	2.3	2.7	dB
Input Return Loss	-	20	-	dB
Output Return Loss	-	25	-	dB
Output Power for 1 dB Compression (P1dB)	19	20	-	dBm
Saturated Output Power	-	21.5	-	dBm
Output Third Order Intercept Point (IP3)	-	33	-	dBm
Supply Current	-	180	190	mA

Test conditions unless otherwise noted: TA=+25 °C, VDD=2.5 V, VSS=-2.5 V, EN=2.5 V, ID=180 mA, Z0=50 Ω

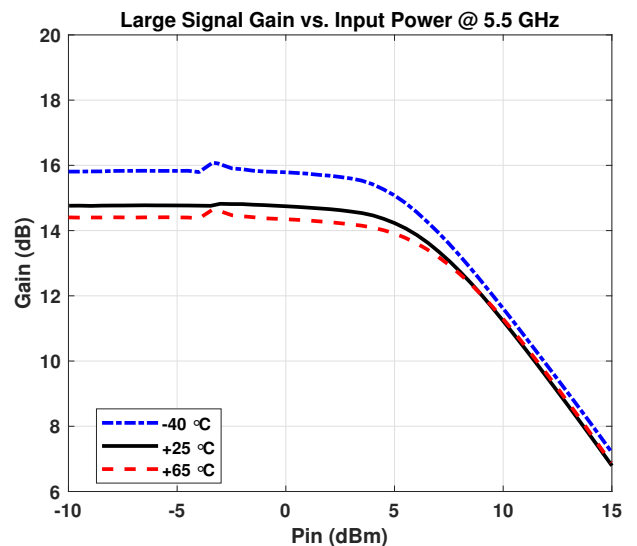
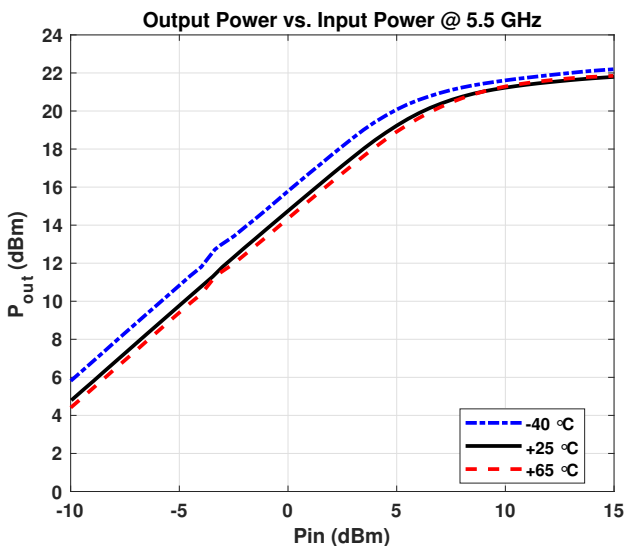
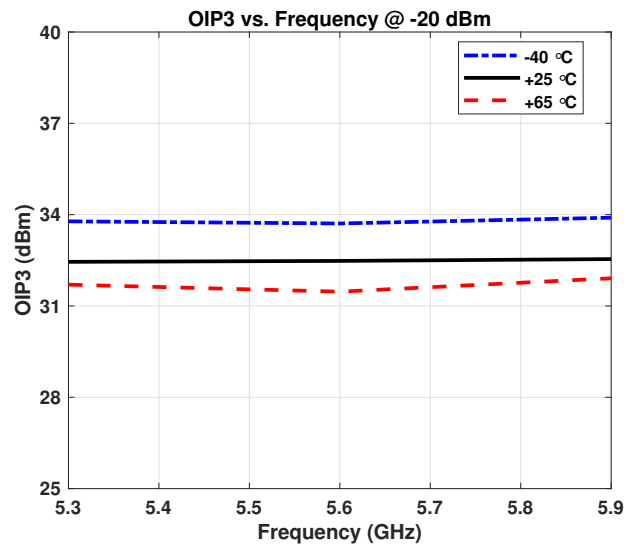
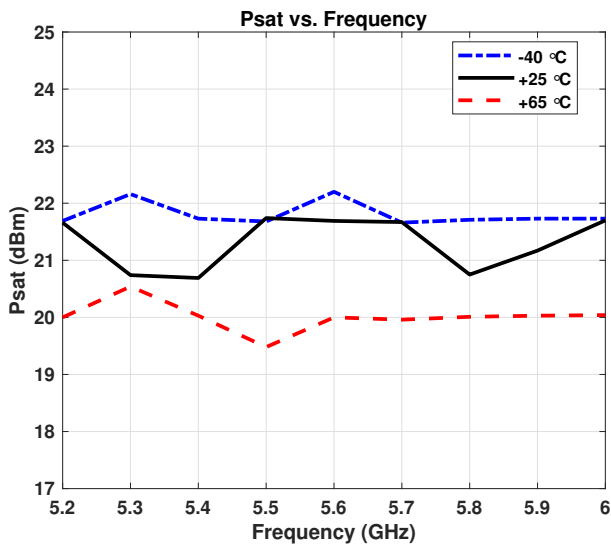
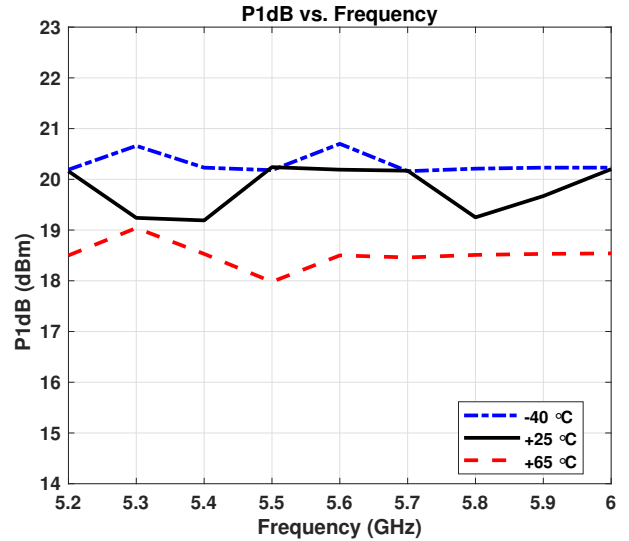
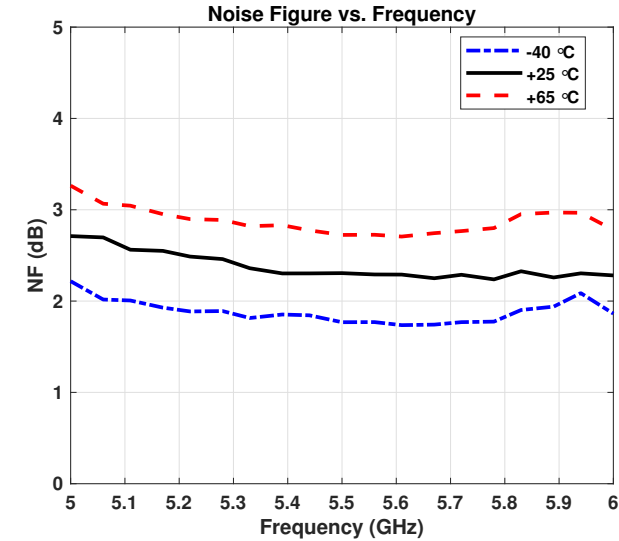
Typical Performance Curves

Test conditions unless otherwise noted: VDD=2.5 V, VSS=-2.5 V, EN=2.5 V

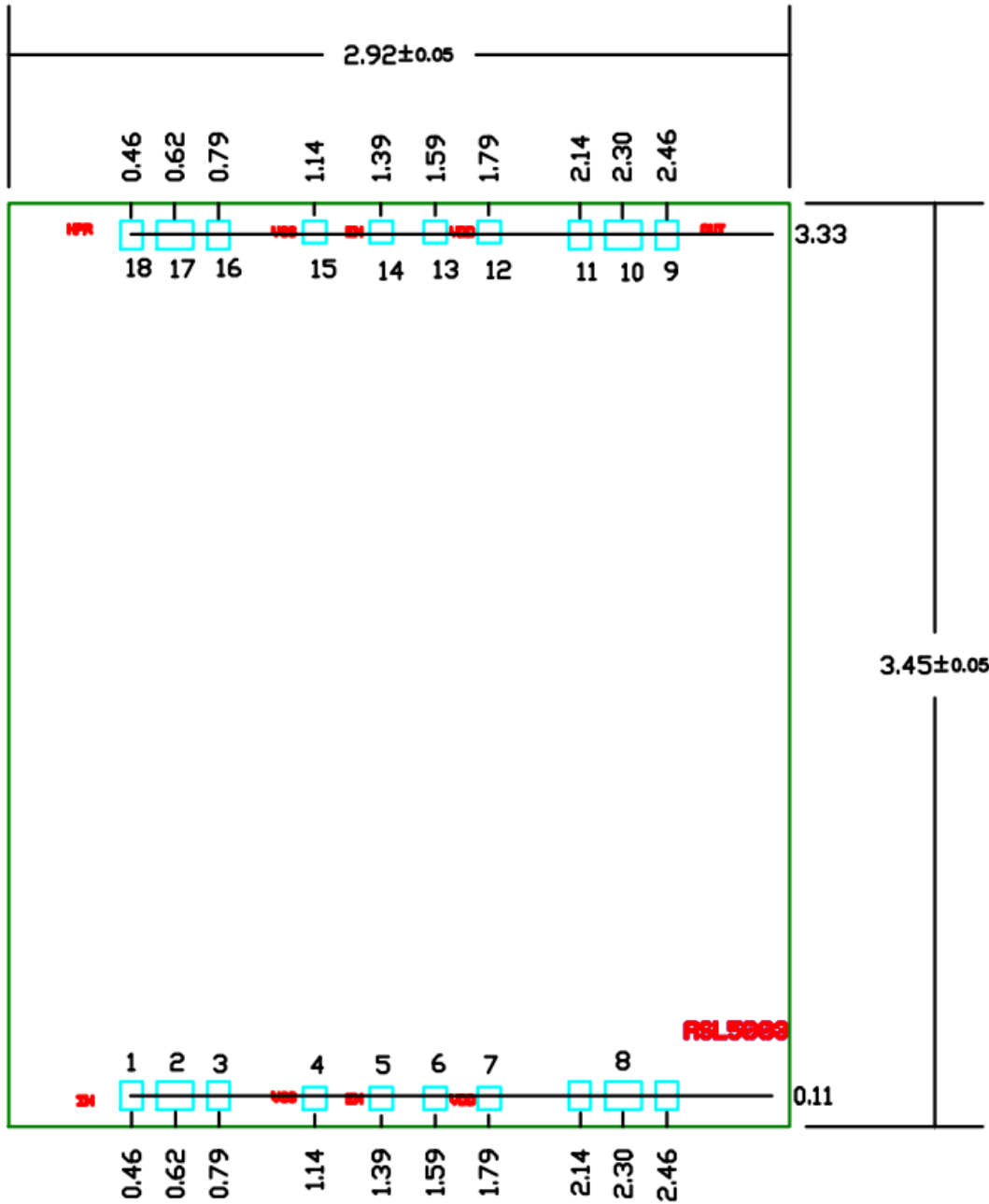


Typical Performance Curves

Test conditions unless otherwise noted: VDD=2.5 V, VSS=-2.5 V, EN=2.5 V



Mechanical Information



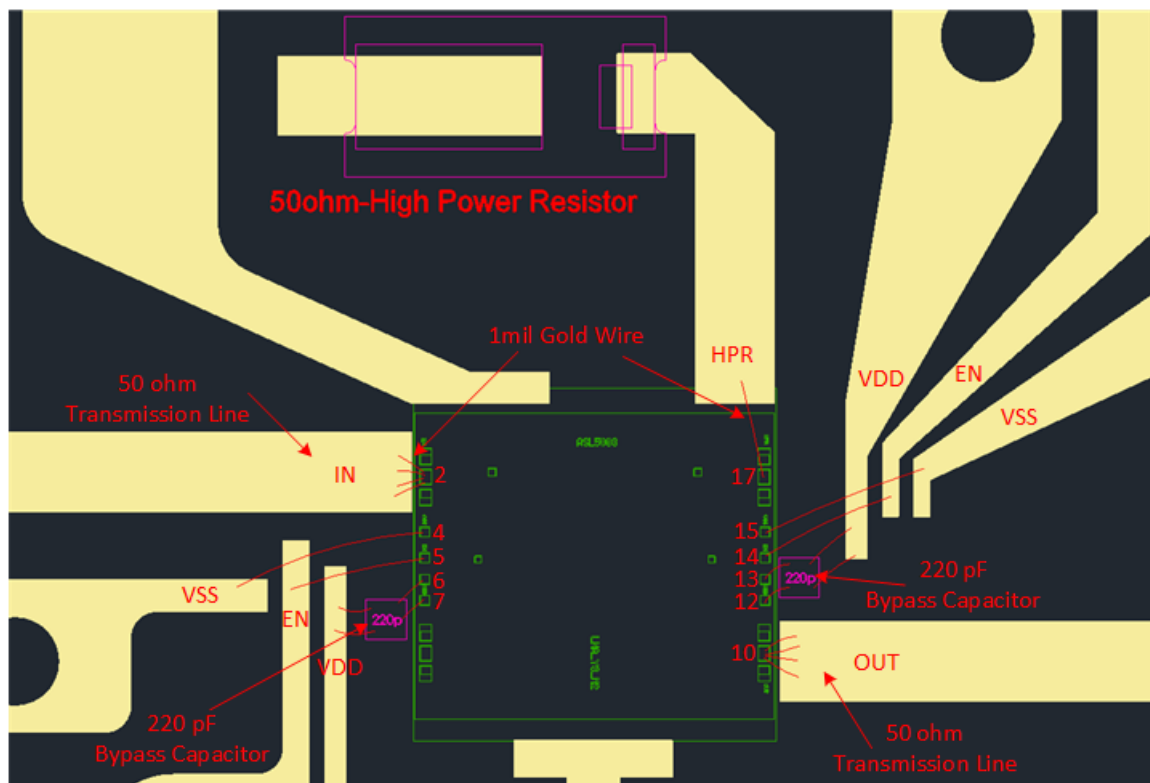
NOTES:

1. ALL DIMENSIONS IN MILLIMETERS
2. DIE THICKNESS IS 100 μ m
3. TYPICAL BOND PAD IS 0.01 mm²
4. BACKSIDE METALLIZATION: GOLD
5. BACKSIDE METAL IS GROUND
6. BOND PAD METALLIZATION: GOLD
7. NO CONNECTION REQUIRED FOR UNLABELED BOND PADS
8. Die Size: OVERALL DIE SIZE ± 50 μ m

Bond Pad Description

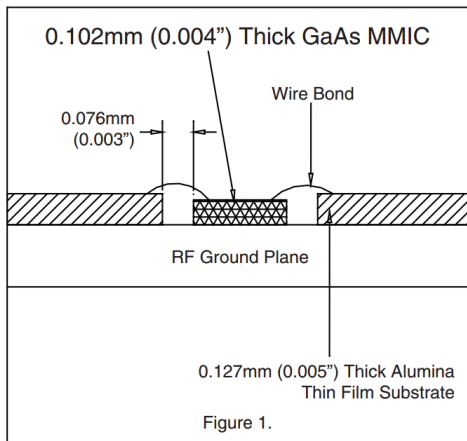
2	RF-IN	This pad is AC coupled and matched to 50 Ohms.
10	RF-OUT	This pad is AC coupled and matched to 50 Ohms.
1,3,8,9,11,16,18,Die bottom	GND	These pads & die bottom are RF/DC ground. The die bottom must be connected to the RF/DC ground. Other pads connections are optional.
6,7,12,13	VDD	Positive Supply Voltage for the amplifier. External bypass capacitors of 220 pF are optional.
4,15	VSS	Negative Supply Voltage for the amplifier.
5,14	EN	This pad is for enabling/disabling of amplifier. (Active High) A digital signal 0/2.5V with minimum current of 2 mA. This pad is pulled down internally.
17	HPR	This pad is for an external 5-W 50 Ohms resistor. (For input RF power of 37 dBm CW)

Assembly Diagram

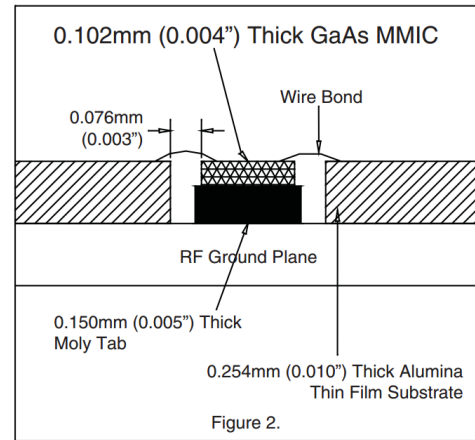


Mounting and Bonding Techniques for Millimeter wave GaAs MMICs

The die should be attached directly to the ground plane eutectically or with conductive epoxy. 50 Ohm Microstrip transmission lines on 0.127mm (5 mil) thick alumina thin film substrates are recommended for bringing RF to and from the chip (Figure 1). If 0.254mm (10 mil) thick alumina thin film substrates must be used, the die should be raised 0.150mm (6 mils) so that the surface of the die is coplanar with the surface of the substrate. One way to accomplish this is to attach the 0.102mm (4 mil) thick die to a 0.150mm (6 mil) thick molybdenum heat spreader (moly-tab) which is then attached to the ground plane (Figure 2). Microstrip substrates should be brought as close to the die as possible in order to minimize bond wire length. Typical die-to-substrate spacing is 0.076mm (3 mils)



The surface of the chip has fragile air bridges and should not be touched with vacuum collet, tweezers, or fingers.



Mounting

The chip is back-metallized and can be die mounted with AuSn eutectic preforms or with electrically conductive epoxy. The mounting surface should be clean and flat.

Eutectic Die Attach: A 80/20 gold tin preform is recommended with a work surface temperature of 255 °C and a tool temperature of 265 °C. When hot 90/10 nitrogen/hydrogen gas is applied, tool tip temperature should be 290 °C. DO NOT expose the chip to a temperature greater than 320 °C for more than 20 seconds. No more than 3 seconds of scrubbing should be required for attachment.

Epoxy Die Attach: Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer's schedule.

Handling Precautions

Follow these precautions to avoid permanent damage.

Storage: All bare dies are placed in either Waffle or Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems. Static Sensitivity: Follow ESD precautions to protect against >± 250V ESD strikes.

Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.

General Handling: Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers.

Wire Bonding

Ball or wedge bond with 0.025 mm (1 mil) diameter pure gold wire is recommended. Thermosonic wire-bonding with a nominal stage temperature of 150 °C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.5 mm (20 mils).



Contact Information

For the latest specifications, additional product information:

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