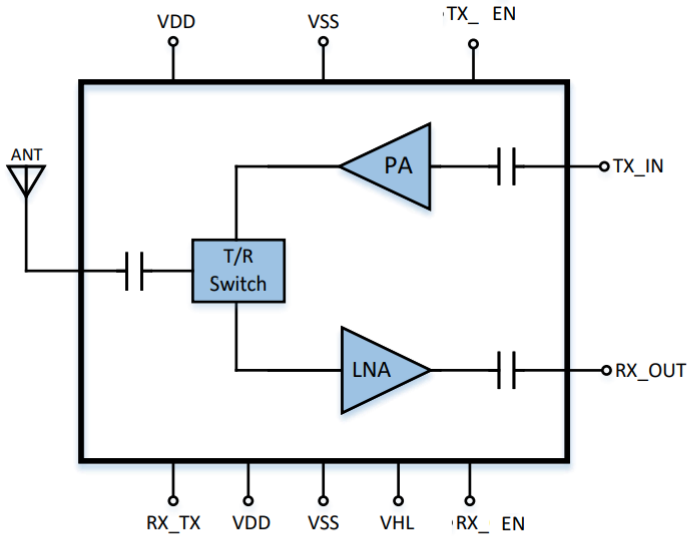
Product Overview

The ASF7002 is a GaAs PHEMT MMIC RF Front End chip which operates from 16 to 18 GHz. The ASF7002 combines a low noise amplifier, power amplifier and one single-pole-double-throw (SPDT) switch; each can be switched on/off with a digital voltage of 0/2.5 V. The receive path has 8dB gain switching feature; which offer 22 dB small signal gain and 3.4 dB noise figure at high gain mode. The measured output IP3 and output P1dB of receiver are 25 dBm and 12 dBm, respectively. The transmit path provides 16 dB of power gain, +24 dBm of saturated output power and 28% power added efficiency. The ASF7002 has a power handling capacity of 0.5W continues wave (CW) into the antenna port, eliminating the need for a limiter. All data is measured with the chip in a 50 Ohm test fixture connected via two 0.025 mm (1mil) diameter bond wires of minimal length 0.51 mm (20mil).

Functional Block Diagram



Key Features

1. Fully integrated, high performance front-end MMIC
2. Integrated DC blocking at RF input/output
3. Enable/Disable mode with digital signal
4. Frequency Range: 16 GHz to 18 GHz
5. RX Gain: 22 dB
6. RX Noise Figure <3.4 dB
7. 8 dB Receiver Gain Switching
8. RX OIP3: 25 dBm
9. TX Power Gain: 16 dB
10. TX Saturated Output Power: 24 dBm
11. TX PAE >28%
12. 50 Ohm Matched Input/output
13. Die Size: 2.97 x 3.72 x 0.1 mm

Applications

1. Communications
2. Electronics Warfare (EW)
3. Commercial and Military Radar
4. Phased Array Antenna

Main Electrical Specifications

Parameter	Min.	Typ.	Max.	Units
Frequency Range	16	-	18	GHz
TX Small Signal Gain	-	0.5	-	dB
TX Psat	-	24.5	-	dBm
RX Gain (at high gain)	-	22	-	dB
RX Noise Figure (at high gain)	-	3.4	-	dB

Electrical Specifications, RX

Parameter	Min.	Typ.	Max.	Units
Frequency Range	16	-	18	GHz
Small Signal Gain (at high gain VHL=2.5V)	-	22	-	dB
Attenuation at Low Gain (VHL=0V)	-	8	-	dB
Noise Figure (at high gain HL=2.5V)	-	3.4	3.6	dB
Input Return Loss	10	12	-	dB
Output Return Loss	10	12	-	dB
Output Power for 1 dB Compression (P1dB)	-	12.5	-	dBm
Saturated Output Power	-	14.5	-	dBm
Output Third Order Intercept (IP3)	-	25	-	dBm
Supply Current	-	55	-	mA

Test conditions unless otherwise noted: TA=+25 °C, VDD=2.5 V, VSS=-2.5 V, EN=2.5 V, ENB=0 V, ID=55 mA, Z0=50 Ω

Electrical Specifications, TX

Parameter	Min.	Typ.	Max.	Units
Frequency Range	16	-	18	GHz
Power Gain	-	16.5	-	dB
Input Return Loss	-	10	-	dB
Saturated Output Power	-	24.5	-	dBm
Power Added Efficiency	-	28	-	%
Supply Current	-	350	-	mA

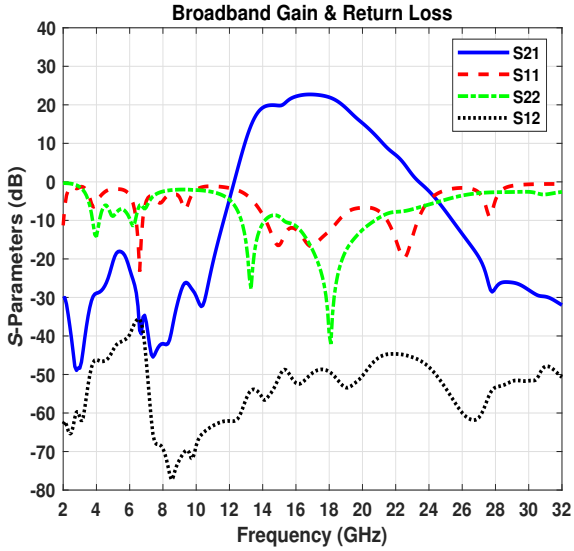
Test conditions unless otherwise noted: TA=+25 °C, VDD=2.5 V, VSS=-2.5 V, EN=0 V, ENB=2.5 V, ID=350 mA, Z0=50 Ω, Pin=8 dBm

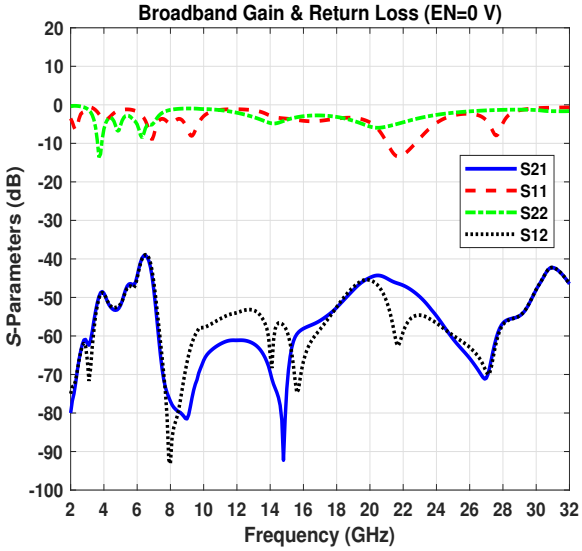
Typical Bias Condition

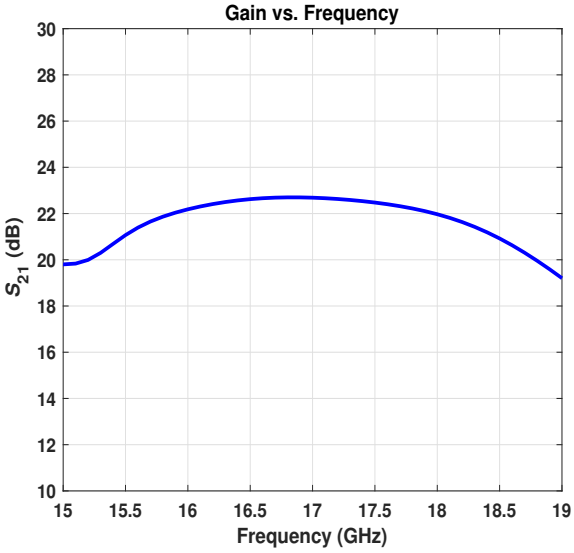
	TX-VDD	RX-VDD	VSS	ENB	EN	VHL	IDq
TX Mode	2.5 V	2.5 V	-2.5 V	2.5 V	0 V	0/2.5 V	10 mA
RX Mode(High Gain)	2.5 V	2.5 V	-2.5 V	0 V	2.5 V	2.5 V	55 mA
RX Mode(Low Gain)	2.5 V	2.5 V	-2.5 V	0 V	2.5 V	0 V	55 mA

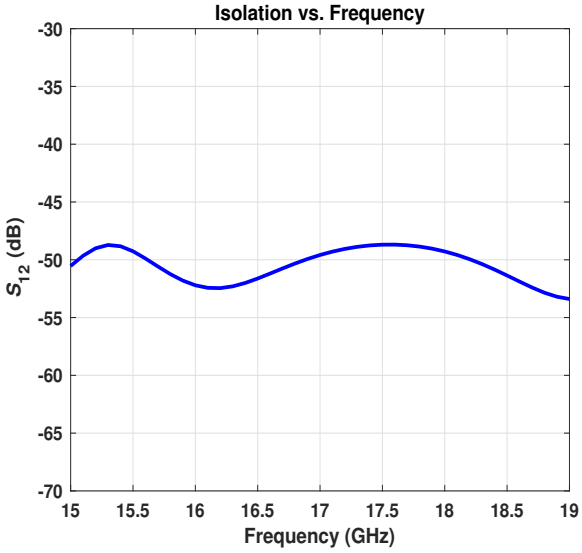
1. NOTE1: Currents are measured at 25 °C
2. NOTE2: The typical operation of amplifier is for supply voltages VSS = -2.5 V, VDD = 2.5 V.

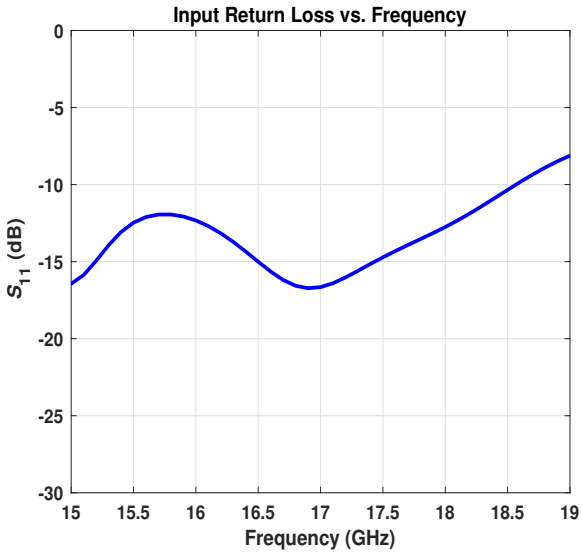
RX Performance Plots (High Gain @ 25 °C)

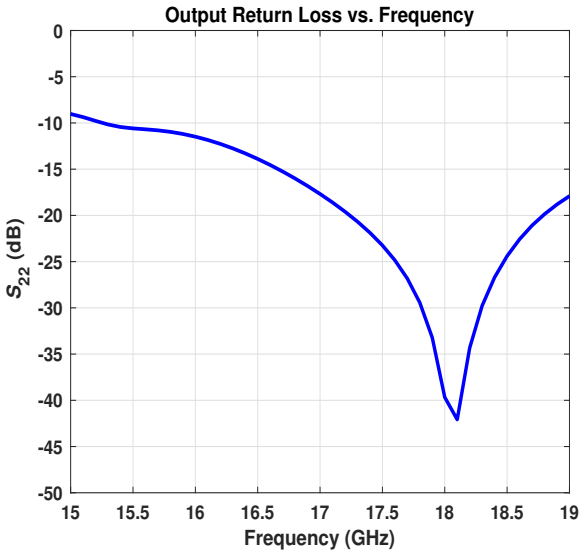




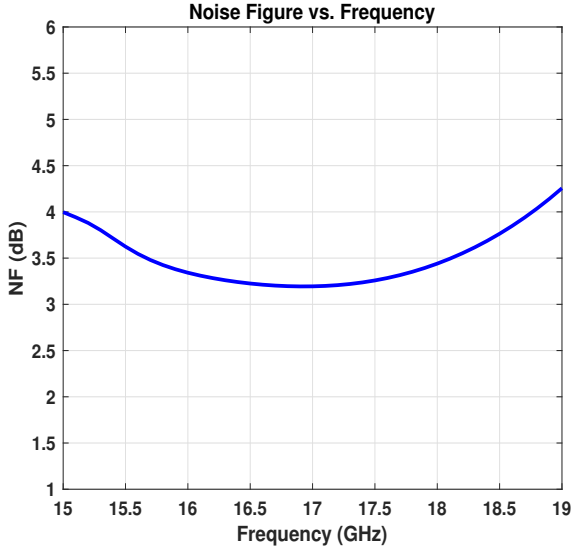


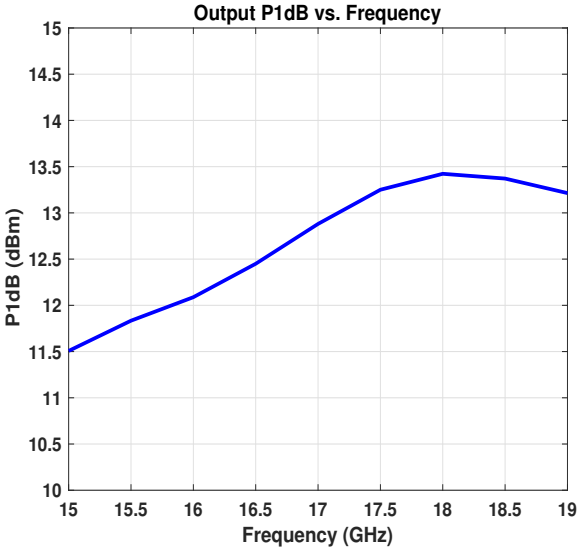


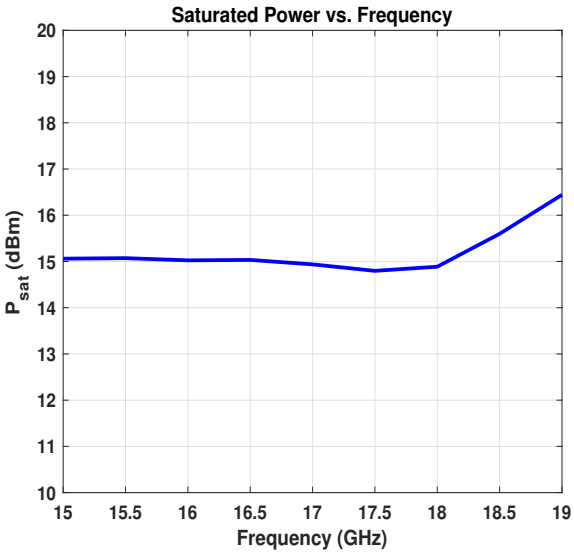


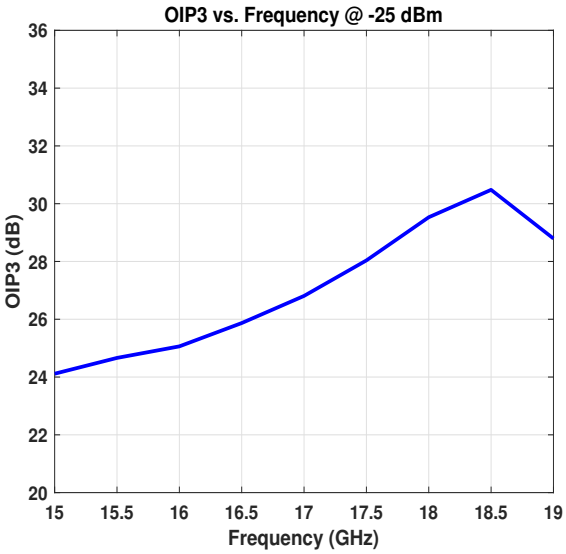


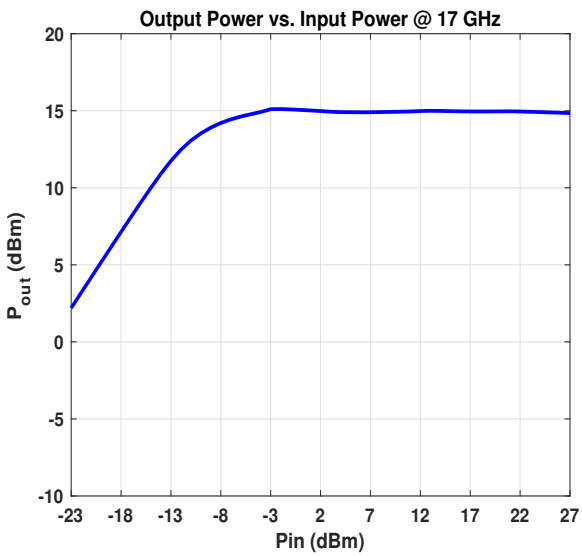
RX Performance Plots (High Gain @ 25 °C)

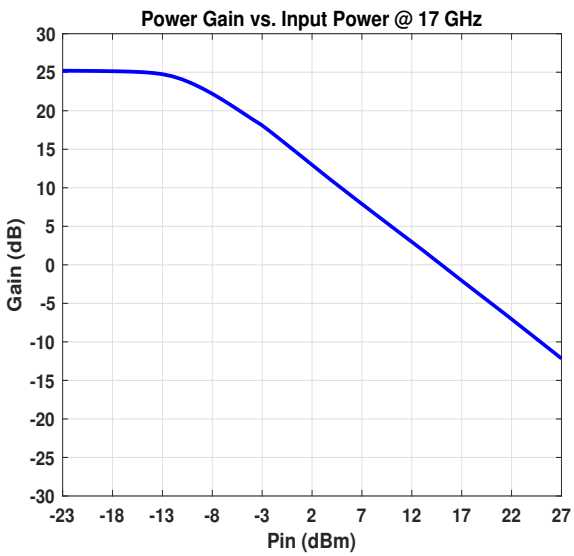




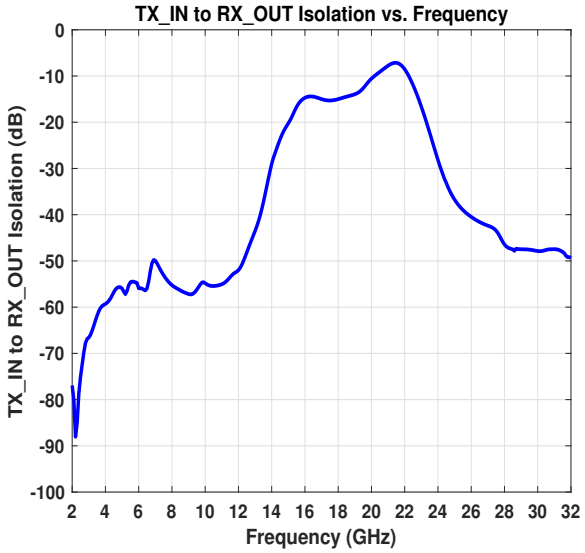




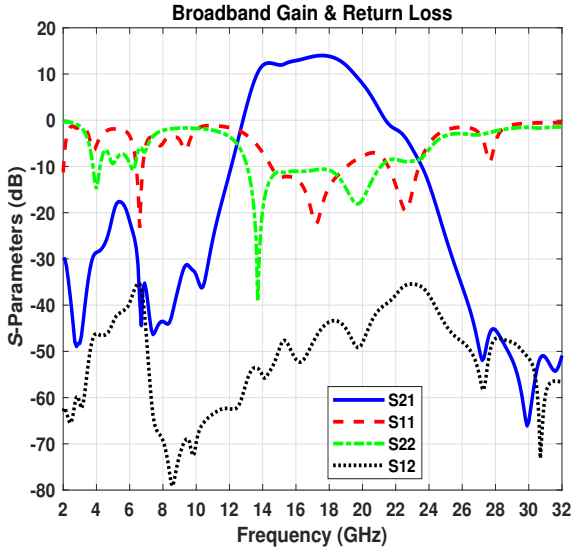


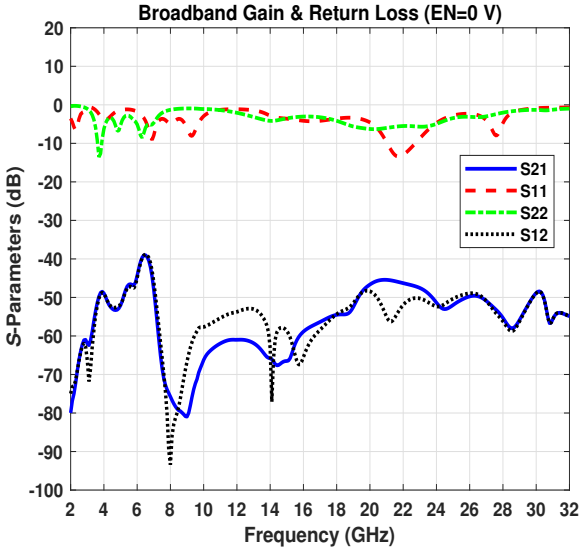


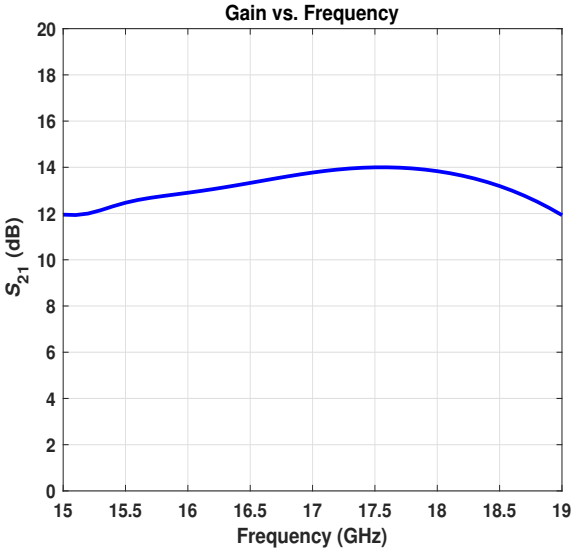
RX Performance Plots (High Gain @ 25 °C)

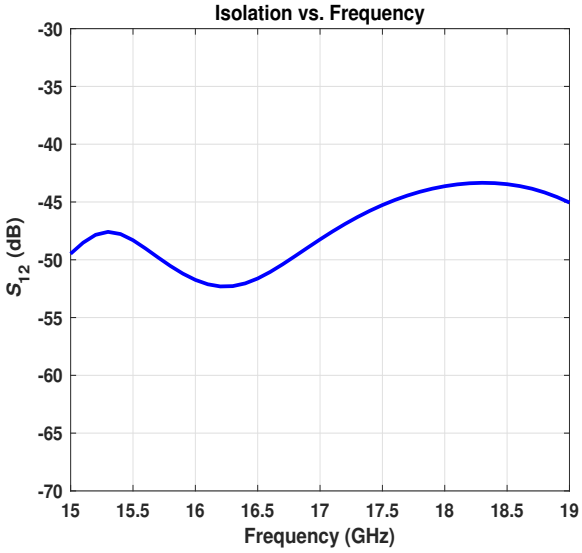


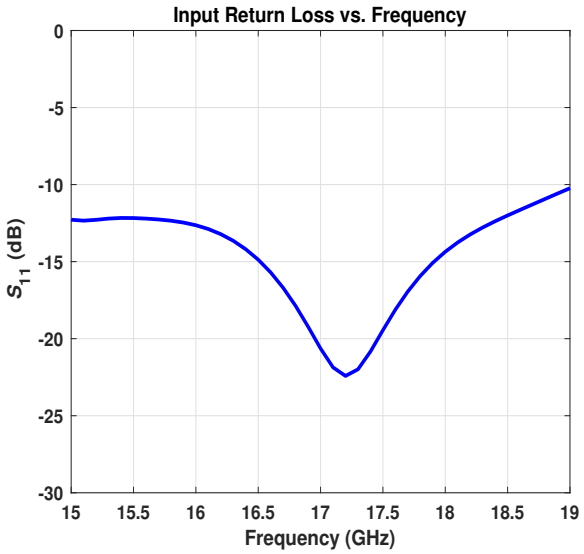
RX Performance Plots (Low Gain @ 25 °C)

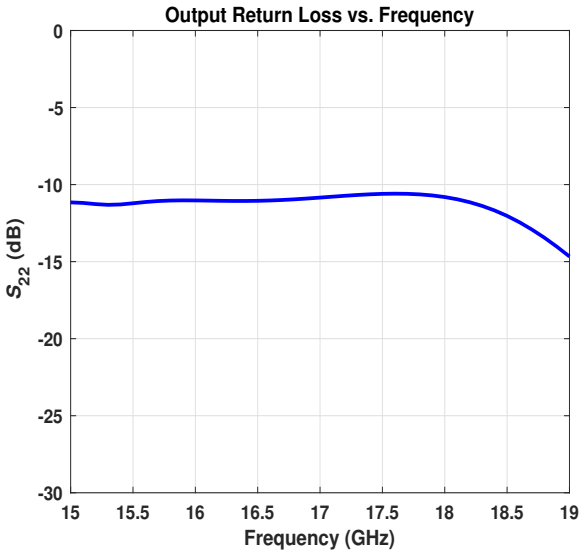




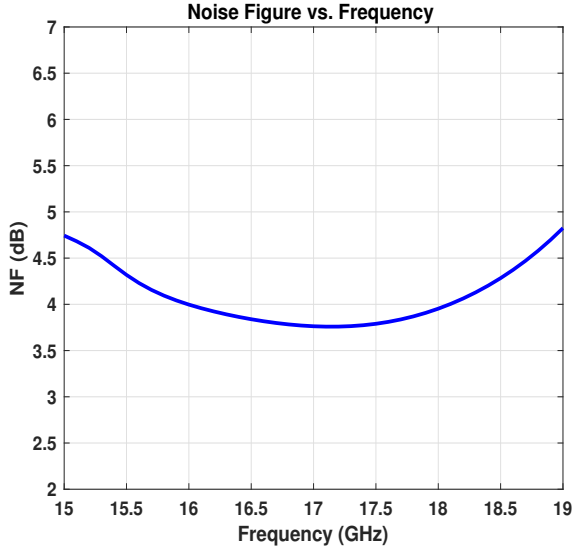


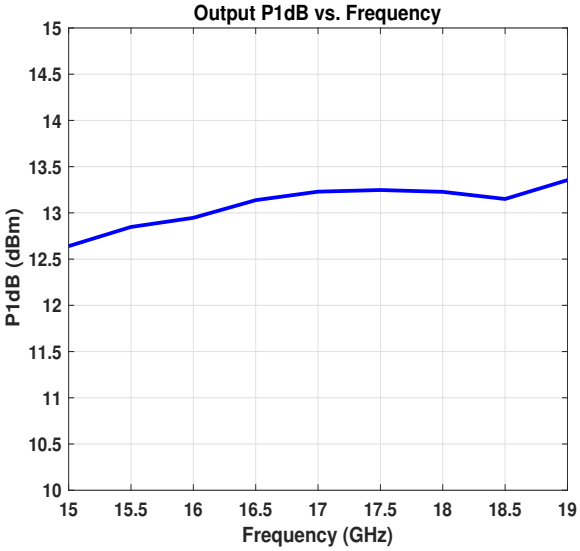


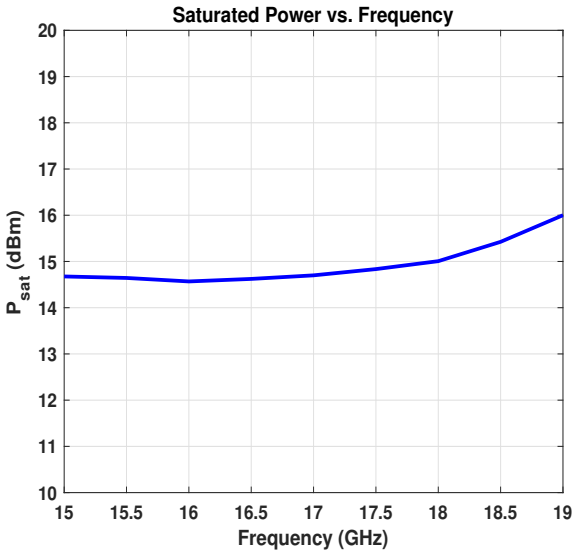


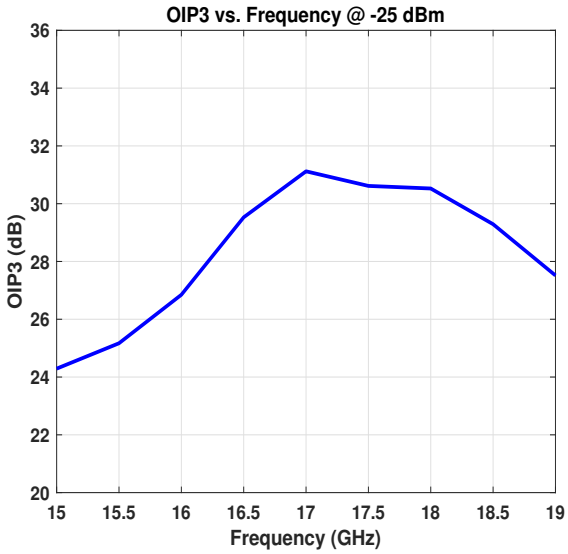


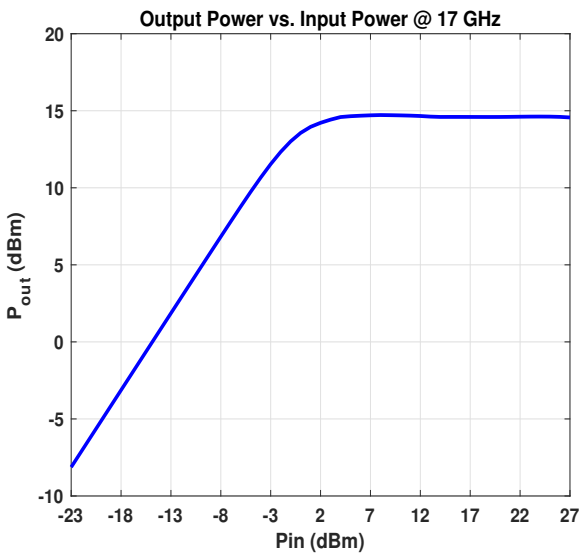
RX Performance Plots (Low Gain @ 25 °C)

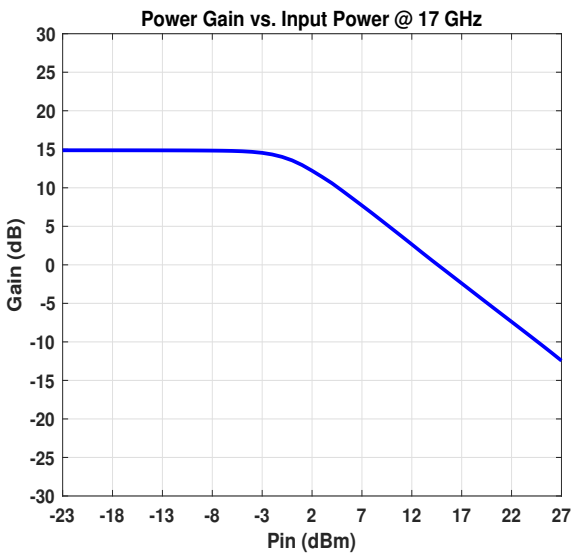




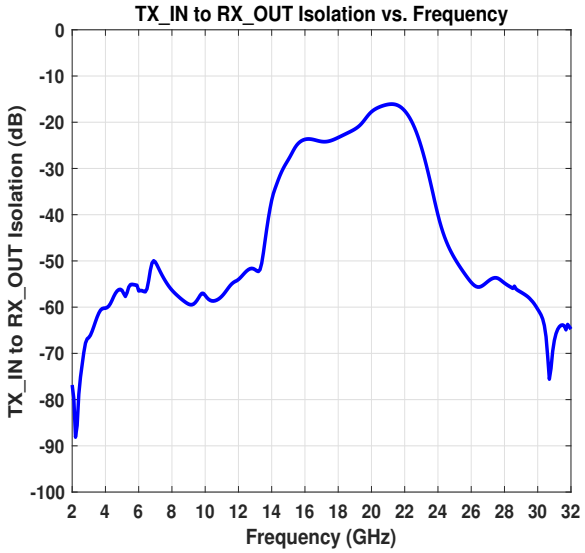




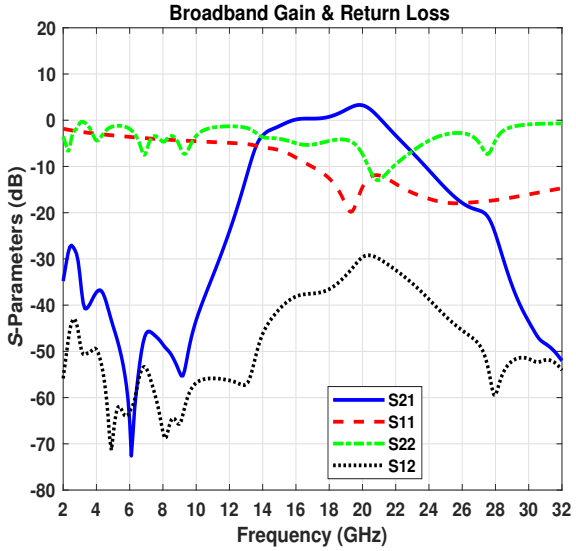


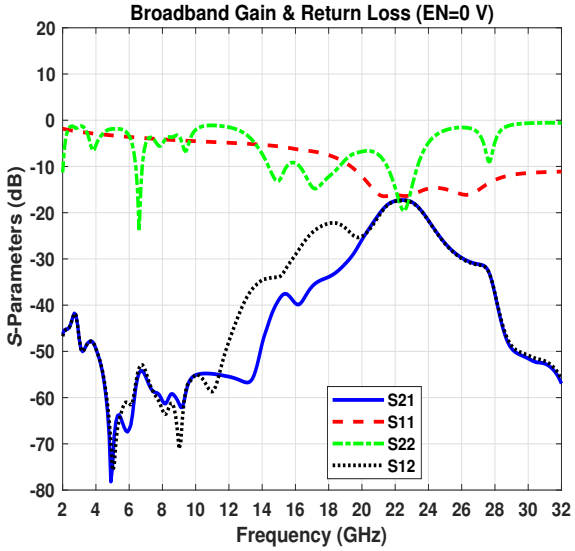


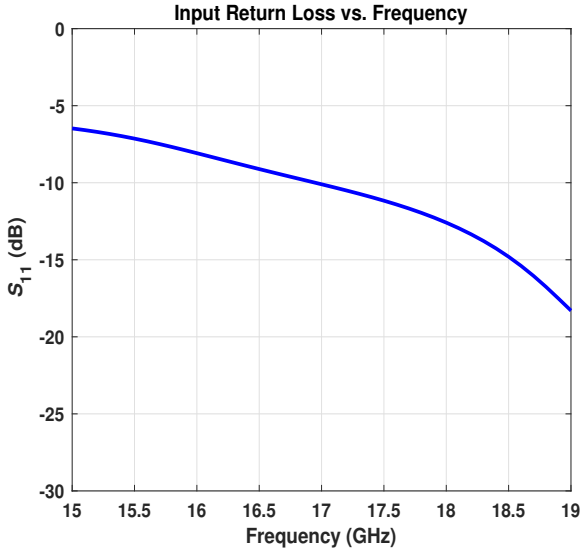
RX Performance Plots (Low Gain @ 25 °C)

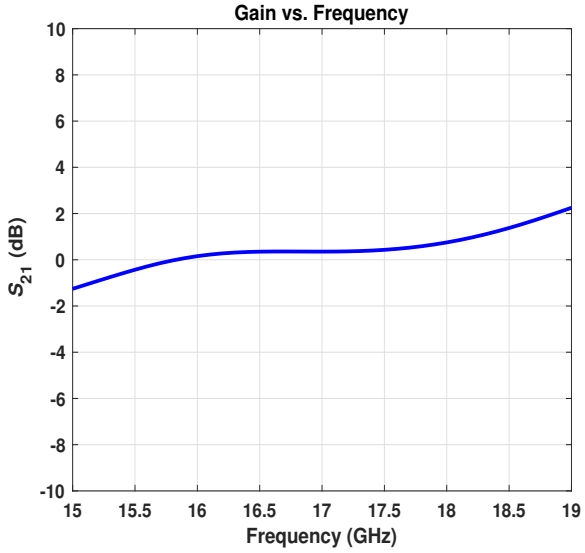


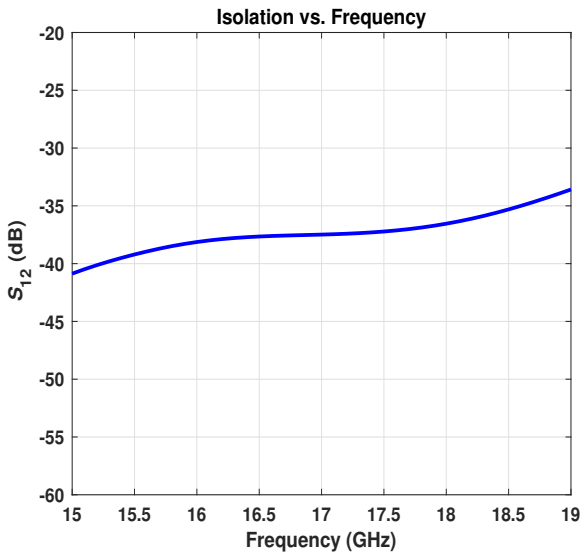
TX Performance Plots – Small Signal (TA = 25 °C)

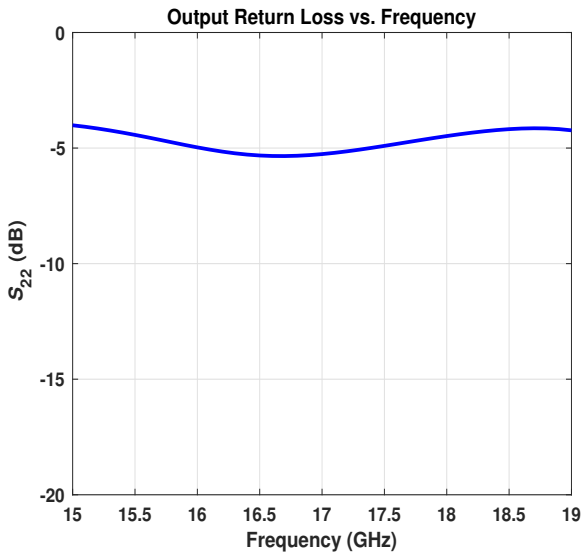






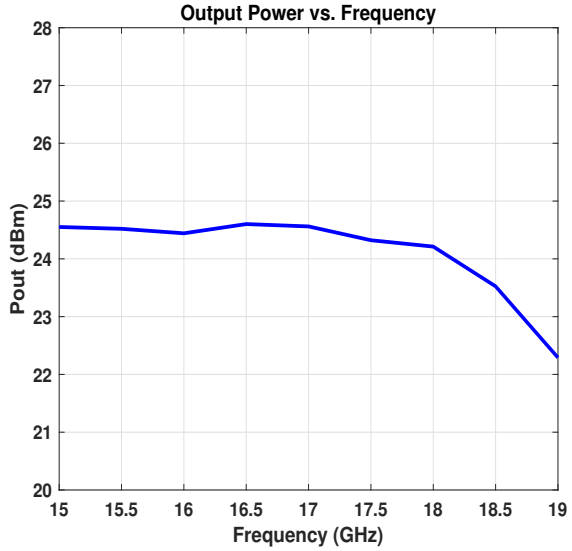


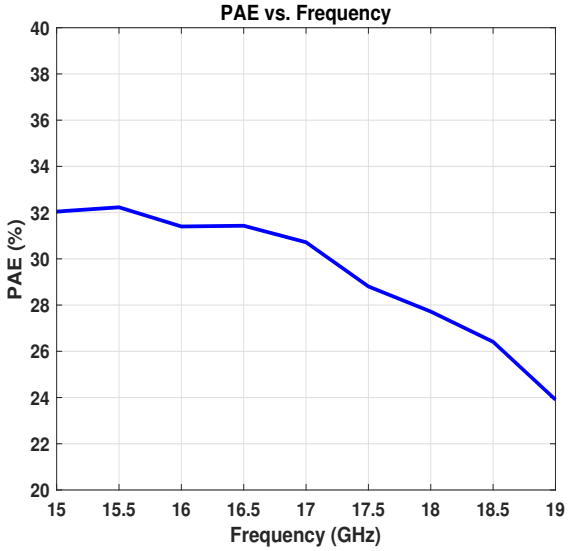


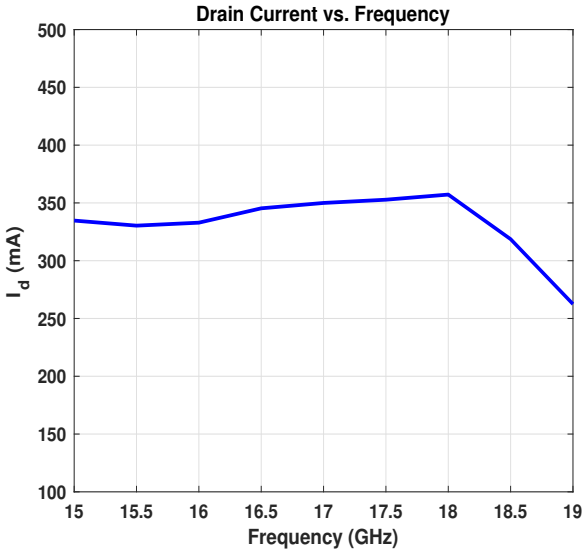


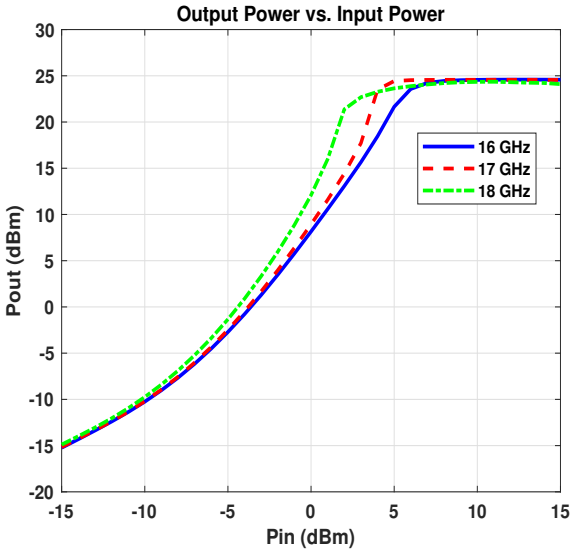
TX Performance Plots – Large Signal

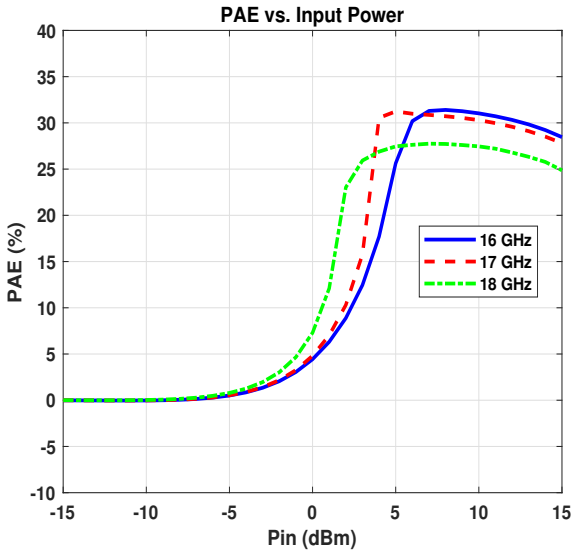
Test conditions unless otherwise noted:TA = 25 °C, Pin = 8 dBm, CW

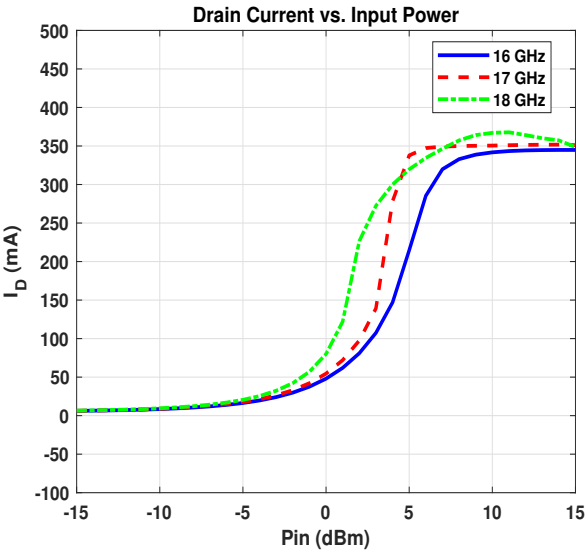






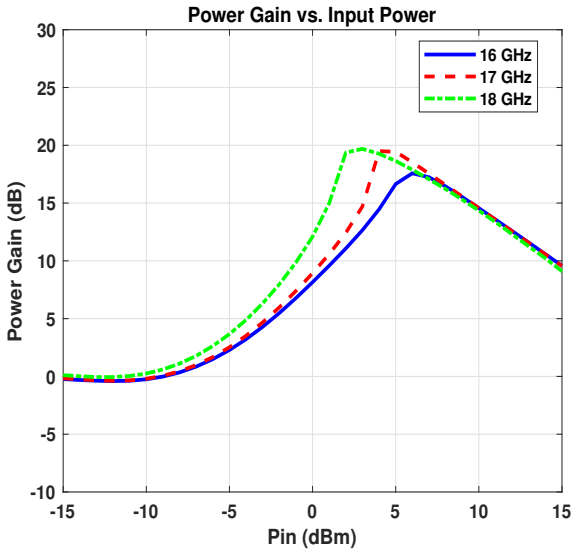


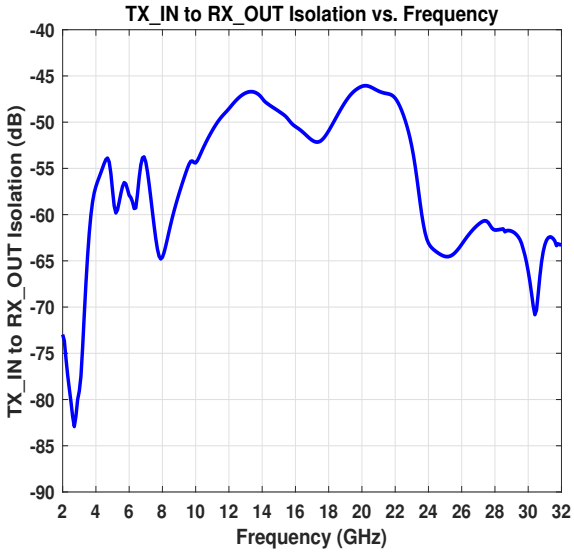




TX Performance Plots – Large Signal

Test conditions unless otherwise noted:TA = 25 °C, Pin = 8 dBm, CW





Absolute Maximum Rating

RX Drain Bias Voltage (VDD)	+3.5 V
Gate Bias Voltage (VSS)	-3.5 V
RX RF Input Power (CW, VDD=2.5 V)	27 dBm
TX RF Input Power (CW, VDD=2.5 V)	15 dBm
Channel Temperature	175 °C
TX Continuous Power Dissipation (T=85 °C)	0.5 W
RX Continuous Power Dissipation (T=85 °C)	0.1 W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

ELECTROSTATIC SENSITIVE DEVICE OBSERVE HANDLING PRECAUTIONS

Bias-up Procedure

RX Mode:

1. Ground The Device
2. Set VSS to -2.5V
3. Set VDD to 2.5V
4. Set VHL to 2.5V (High Gain) or 0V (Low Gain)
5. Set ENB to 0V
6. Set EN to 2.5V
7. Apply RF Input Signal

TX Mode:

1. Ground The Device
2. Set VSS to -2.5V
3. Set VDD to 2.5V
4. Set VHL to 2.5V or 0V
5. Set EN to 0V
6. Set ENB to 2.5V
7. Apply RF input Signal

Bias-down Procedure

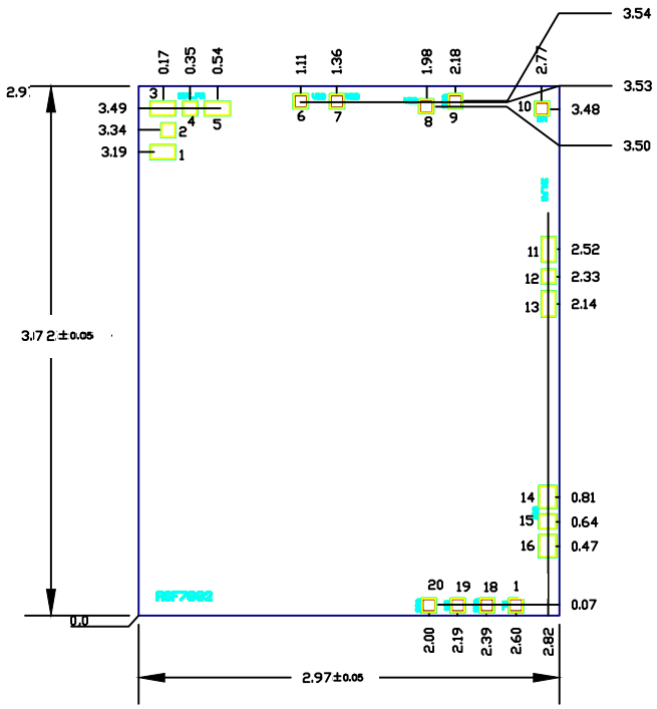
RX Mode:

1. Remove RF Input Signal
2. Set EN to 0V
3. Set VHL to 0V
4. Set VDD to 0V
5. Set VSS to 0V

TX Mode:

1. Remove RF Input Signal
2. Set ENB to 0V
3. Set VHL to 0V
4. Set VDD to 0V
5. Set VSS to 0V

Mechanical Information



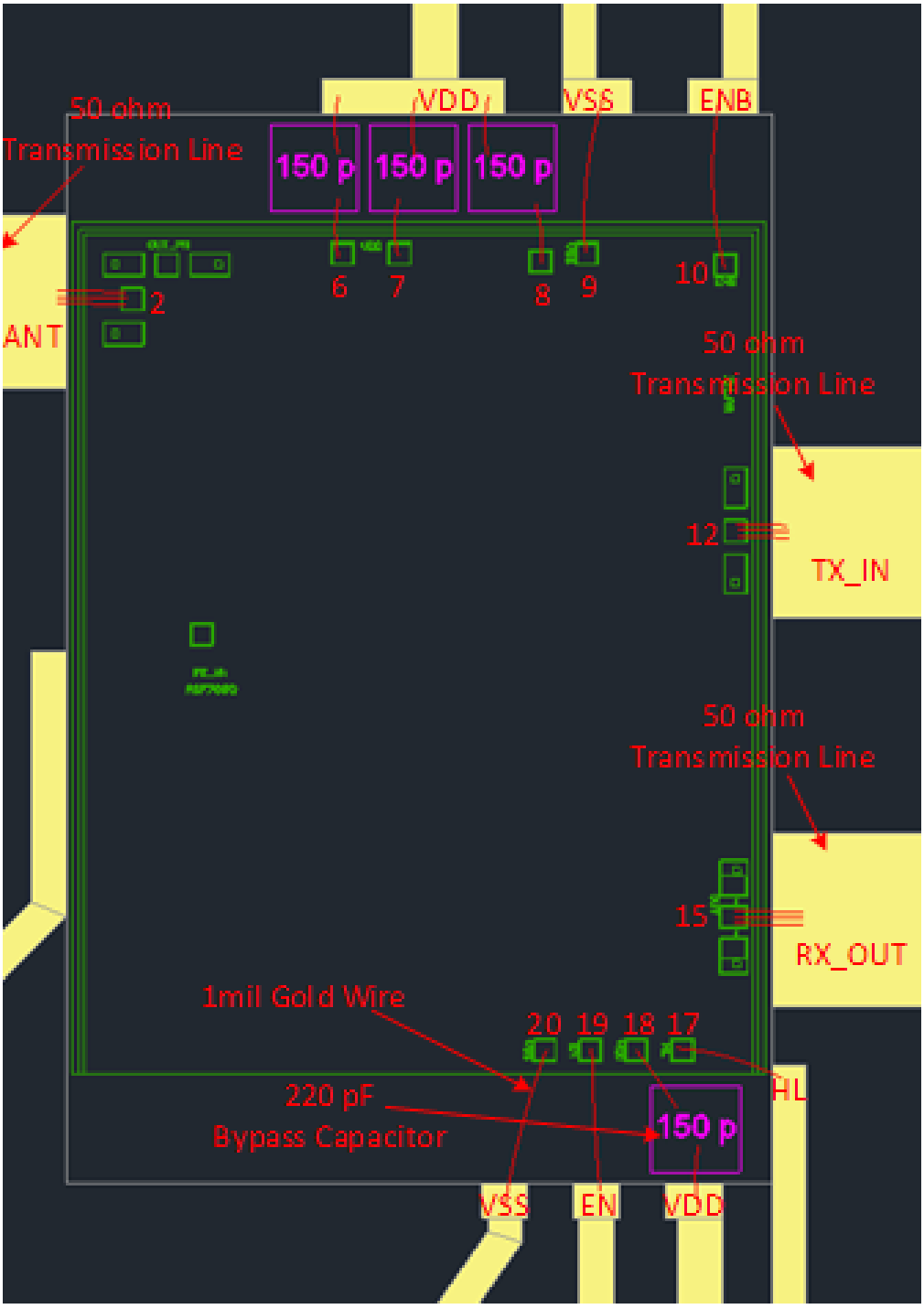
NOTES:

1. ALL DIMENSIONS IN MILLIMETERS
2. DIE THICKNESS IS 100 µm
3. TYPICAL BOND PAD IS 0.01 mm2
4. BACKSIDE METALLIZATION: GOLD
5. BACKSIDE METAL IS GROUND
6. BOND PAD METALIZATION: GOLD
7. NO CONNECTION REQUIRED FOR UNLABELED BOND PADS
8. OVERALL DIE SIZE ±50 µm

Bond Pad Description

12	TX-IN	This pad is AC coupled and matched to 50 Ohms.
2,4	ANT	This pad is AC coupled and matched to 50 Ohms.
15	RX-OUT	This pad is AC coupled and matched to 50 Ohms.
1,3,5,11,13,14,16,Die bottom	GND	These pads & die bottom are RF/DC ground. The die bottom must be connected to the RF/DC ground. Other pads connections are not required.
6,7,8,18	VDD	TX Positive Supply Voltage. External Bypass Capacitors 150 pF are required.
19	EN	This pad is for enabling/disabling of LNA. (Active High) A digital signal 0/2.5V with minimum current of 2 mA. This pad is pulled down internally.
10	ENB	This pad is for enabling/disabling of PA. (Active High) A digital signal 0/2.5V with minimum current of 2 mA. This pad is pulled down internally.
17	VHL	This pad is for high/low gain mode of LNA. (Active High) A digital signal 0/2.5V with minimum current of 2 mA. Floating Pad is not allowed.
9, 20	VSS	Negative Supply Voltage for the amplifiers.

Assembly Diagram



Mounting and Bonding Techniques for Millimeter wave GaAs MMICs

The die should be attached directly to the ground plane eutectically or with conductive epoxy. 50 Ohm Microstrip transmission lines on 0.127mm (5 mil) thick alumina thin film substrates are recommended for bringing RF to and from the chip (Figure 1). If 0.254mm (10 mil) thick alumina thin film substrates must be used, the die should be raised 0.150mm (6 mils) so that the surface of the die is coplanar with the surface of the substrate. One way to accomplish this is to attach the 0.102mm (4 mil) thick die to a 0.150mm (6 mil) thick molybdenum heat spreader (moly-tab) which is then attached to the ground plane (Figure 2). Microstrip substrates should be brought as close to the die as possible in order to minimize bond wire length. Typical die-to-substrate spacing is 0.076mm (3 mils)

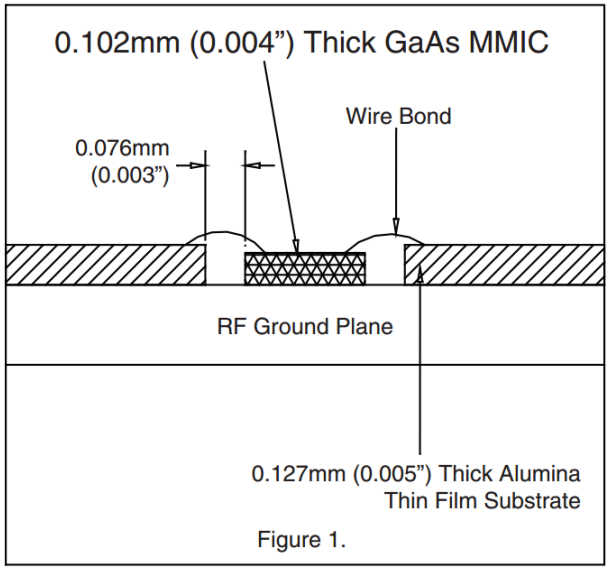


Figure 1.

Handling Precautions

Follow these precautions to avoid permanent damage.
Storage: All bare dies are placed in either Waffle or Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.
Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.
Static Sensitivity: Follow ESD precautions to protect against >± 250V ESD strikes.
Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.
General Handling: Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers.

The surface of the chip has fragile air bridges and should not be touched with vacuum collet, tweezers, or fingers.

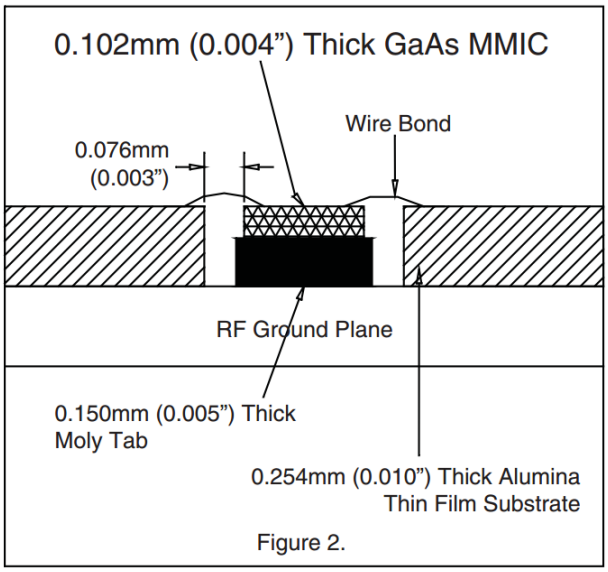


Figure 2.

Mounting

The chip is back-metallized and can be die mounted with AuSn eutectic preforms or with electrically conductive epoxy. The mounting surface should be clean and flat.
Eutectic Die Attach:A 80/20 gold tin preform is recommended with a work surface temperature of 255 °C and a tool temperature of 265 °C. When hot 90/10 nitrogen/hydrogen gas is applied, tool tip temperature should be 290 °C. DO NOT expose the chip to a temperature greater than 320 °C for more than 20 seconds. No more than 3 seconds of scrubbing should be required for attachment.
Epoxy Die Attach: Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer's schedule.

Wire Bonding

Ball or wedge bond with 0.025 mm (1 mil) diameter pure gold wire is recommended. Thermosonic wirebonding with a nominal stage temperature of 150 °C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.5 mm (20 mils).

Contact Information

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