ASPGC4X20

Quadruple, Positive Voltage Low noise, 120V/µs, Rail-to-Rail Adjustable Output RF Amplifier Gate Bias Control & Monitoring

Features

- **Internal Op-Amp -3dB Band-Width: 60MHz (90MHz with FST_EN), A_V = 1**
- **Slew Rate: 70V/µS (120V/µS with FST_EN)**
- **Wide Supply Range: 2.5V to 12V**
- **Output Current: 20mA (45mA with FST_EN)**
- **Four Separated Output Array**
  - **Output Swings Rail-to-Rail**
  - **Output Offset Voltage, Rail-to-Rail: 5mV Max**
  - **Low Output Noise: 20µvrms (10Hz to 100kHz)**
  - **Power Supply Rejection: 75dB Typ.**
  - **Programmable Soft-Start**
  - **Operating Temperature Range: –40°C to 125°C**
  - **Low Profile (5mm x 11mm x 0.75mm) QFN Package**

Applications

- Power Management unit
- RF Amplifier Gate Control and Monitoring
- RF Transceivers

Description

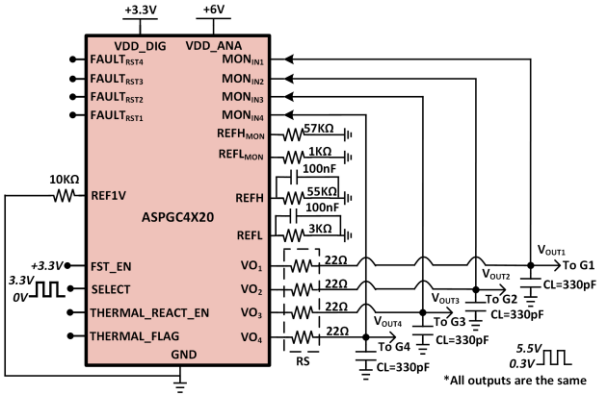
The ASPGC4X20 is a quad negative gate control and monitor with up to 120 V/µS output slew rate. The outputs have been driven with four unity– gain amplifiers with a gain-bandwidth of 60MHz and a 20mA (40mA with FST_EN) output current fit the requirements of high-performance RF bias boards. The ASPGC4X20 has a digital positive SELECT input and quad rail to rail outputs that swing within 100mV of GND and 300mV of VDD_ANA rail to maximize the signal dynamic range in low voltage applications.

The ASPGC4X20 has low output RMS noise and precision output voltage levels that are adjusted with only two resistors. It has four precision monitoring blocks with adjustable power good range and four output flags.

The ASPGC4X20 maintains its performance with a VDD_ANA voltage from 3V to 12V and a VDD_DIG voltage from 2V to 5V. The Input digital SELECT levels are GND and VDD_DIG and the output voltage and monitoring levels can be set between GND and VDD_ANA.

Typical Application

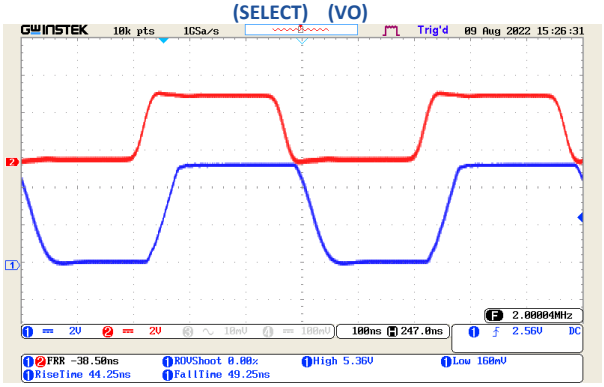
Quadrative Gate Control and monitoring



Large signal

0.3 V to 5.5 V Step @ VDD_ANA=6 V, VDD_DIG = +3.3 V FAST_EN = 1 RS = 22 Ω, CL = 330 pF, RL = 1 KΩ

(SELECT) (VO)



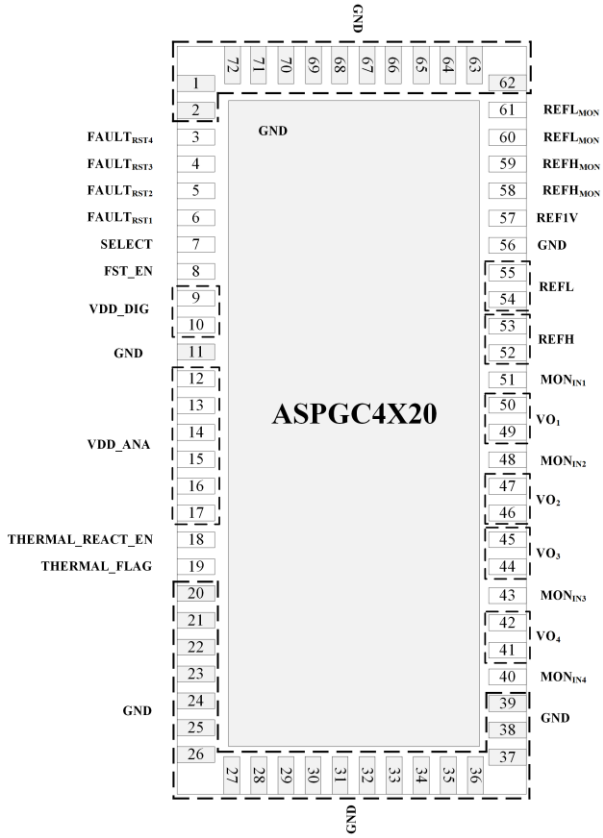
Absolute Maximum Rating

VDD_ANA.....-0.5 V to 13 V
VDD_DIG ..... -0.5 V to 5.5 V
GND ..... 0 V
FAULT_RSTx..... -0.5 V to VDD_DIG +0.5 V
SELECT. ..... -0.5 V to VDD_DIG +0.5 V
FST_EN..... -0.5 V to VDD_DIG +0.5 V
THERMAL_REACT_EN.....-0.5 V to VDD_DIG +0.5 V
THERMAL_FLAG.....-0.5 V to VDD_DIG +0.5 V
VOx , MON_INx..... -0.5 V to VDD_ANA+0.5 V
REFH, REFL..... -0.5 V to VDD_ANA+0.5 V
REFH_MON, REFL_MON.....-0.5 V to VDD_ANA+0.5 V
REF1V..... -0.5 V to 5 V
Maximum Junction Temperature..... 250 °C

Recommended Pin Voltage Range

VDD_ANA .....3 V to 13 V
VDD_DIG ..... 2.5 V to 5.5 V
GND ..... 0 V
FAULT_RSTx..... Digital OUT (0 to VDD_DIG)
SELECT. ..... Digital IN (0 to VDD_DIG)
FAST_EN..... Digital IN (0 to VDD_DIG)
THERMAL_REACT_EN..... Digital IN (0 to VDD_DIG)
THERMAL_FLAG..... Digital OUT (0 to VDD_DIG)
VOx ..... +0.1 V to VDD_ANA -0.3 V
MON_INx .....+0.1 V to VDD_ANA -0.3 V
REFH, REFL..... +0.1 V to VDD_ANA -0.3 V
REFH_MON, REFL_MON..... 0 V to VDD_ANA -0.3 V
REF1V..... Analog OUT (+1 V)
Maximum Junction Temperature..... 150 °C

Pin Configuration



Electrical Characteristics

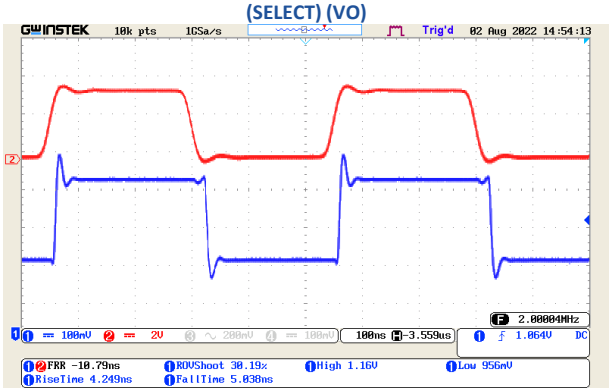
T_A = 25 °C, VDD_DIG = 3.3 V, VDD_ANA = 4.5 V, R_{REFH} = 33.8 KΩ, R_{REFL} = 3 KΩ, R_{REF1V} = 10 KΩ, R_{HMON} = 39.1 KΩ, R_{LMON} = 2 KΩ, R_S=22 Ω

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNITS
$VREF_{1V}$		R_{REF1V}=10K		1.05		V
$VREF_H$				3.57		V
$VREF_L$				0.313		V
$VREF_{HMON}$				4.07		V
$VREF_{LMON}$				0.21		V
$IREF_L$				104.3		µA
$IREF_H$				105.6		µA
$IREF_{LMON}$				105		µA
$IREF_{HMON}$				104.1		µA
V_O		Select = High Select = Low		3.59 0.32		V V
$I_{IN-SELECT}$		Select = High Select = Low		100 0		uA uA
V_{OL}	Output Voltage Lower-Level Swing	No Load I_{Load} = ±20mA		0.1 0.1		V V
V_{OH}		No Load I_{Load} = ±20mA		4.15 4.15		V
I_{SH}	Output Short Circuit	to GND, FST_EN=Low to VDD_ANA , FST_EN= Low to GND, FST_EN=High to VDD_ANA , FST_EN= High		28 34 48 58		mA
I_{DD-Dig}	Digital Supply Current	No Load		1		mA
I_{VSS}	Analog Supply Current	No Load, FST_EN=Low No Load, FST_EN=High		37 58		mA
$V_{SELECTH}$	Select Digital High Level			2.2		V
$V_{SELECTL}$	Select Digital Low Level			1.48		V
$t_{SEL-VOLH}$	Select command delay to output V_O 10% (Low to High)	FST_EN = High, C_L = 330pF FST_EN = Low, C_L = 330pF FST_EN = High, C_L = 20pF FST_EN = Low, C_L = 20pF		10 15 4 6		ns ns ns ns
$t_{SEL-VOHL}$	Select command delay to output V_O 10% (High to Low)	FST_EN = High, C_L = 330pF FST_EN = Low, C_L = 330pF FST_EN = High, C_L = 20pF FST_EN = Low, C_L = 20pF		23 25 17 21		ns ns ns ns
t_R	Rising time 0.5V to 4V 10% to 90%	FST_EN = High, C_L = 330pF FST_EN = Low, C_L = 330pF FST_EN = High, C_L = 20pF FST_EN = Low, C_L = 20pF		39 59 27 47		ns ns ns ns
t_F	Falling time 4V to 0.5V 90% to 10%	FST_EN = High, C_L = 330pF FST_EN = Low, C_L = 330pF FST_EN = High, C_L = 20pF FST_EN = Low, C_L = 20pF		40 61 30 50		ns ns ns ns
Slew rate	Slew rate	FST_EN = High, C_L = 330pF FST_EN = Low, C_L = 330pF FST_EN = High, C_L = 20pF FST_EN = Low, C_L = 20pF		90 60 115 70		V/µs

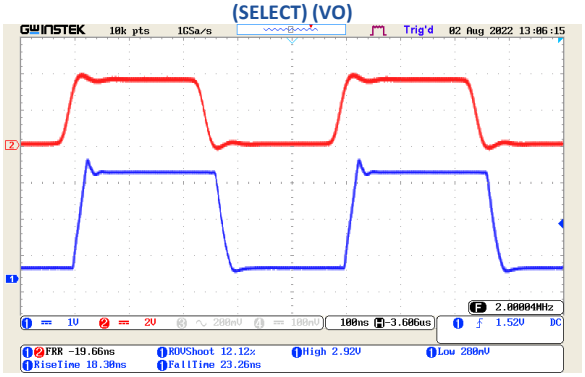
t_{DPG}		Power good Power Bad		82 1000		ms ns
VOS_{MH}	REFH/L_{MON} to MON_{IN} offset voltage to remove PG flag			±1.5		mV
MON_{HYST}				28		mV
$PSRR_{VDD\_ANA}$		VSS = 4V , 12V		81		dB
$PSRR_{DIG}$		VDD_DIG = 2V , 5V		95		dB

Gate Control Typical Performance Characteristics TA = 25◦ unless otherwise noted

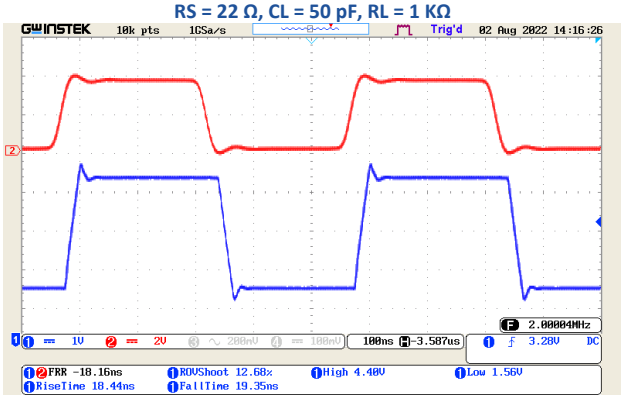
small signal
1 V to 1.2 V Step @ VDD_ANA=4.5 V, VDD_DIG = +3.3 V FAST_EN = 0 RS = 22 Ω, CL = 50 pF, RL = 1 KΩ
(SELECT) (VO)



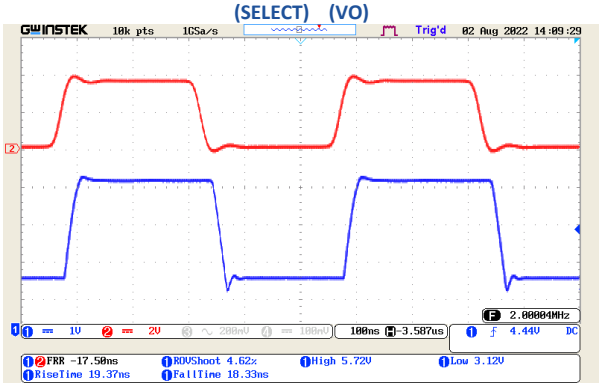
Large signal
0.3 V to 3 V Step @ VDD_ANA=4.5 V, VDD_DIG = +3.3 V FAST_EN = 1 RS = 22 Ω, CL = 50 pF, RL = 1 KΩ
(SELECT) (VO)



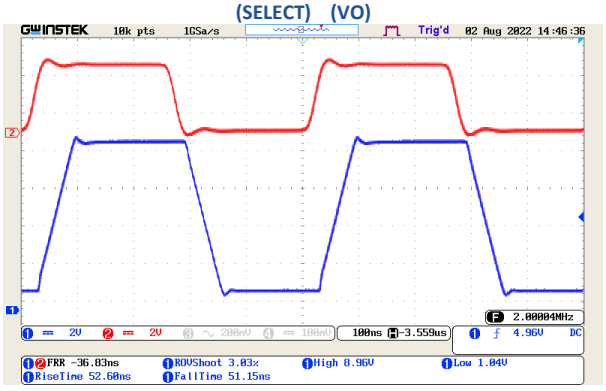
Large signal
+1.5 V to +4.5 V Step @ VDD_ANA=+6 V, VDD_DIG = +3.3 V FAST_EN = 1
RS = 22 Ω, CL = 50 pF, RL = 1 KΩ



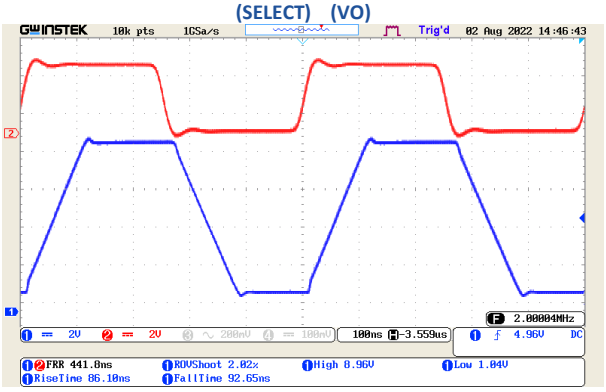
Large signal
3 V to 5.7 V Step @ VDD_ANA=+6 V, VDD_DIG = +3.3 V FAST_EN = 1 RS = 22 Ω, CL = 50 pF, RL = 1 KΩ
(SELECT) (VO)



large signal
1 V to 9 V Step @ VDD_ANA=10 V, VDD_DIG = +3.3 V FAST_EN = 1 RS = 22 Ω, CL = 50 pF, RL = 1 KΩ
(SELECT) (VO)

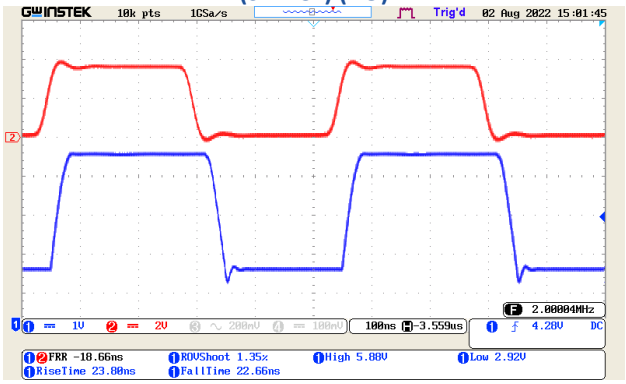


large signal
1 V to 9 V Step @ VDD_ANA=10 V, VDD_DIG = +3.3 V FAST_EN = 0 RS = 22 Ω, CL = 50 pF, RL = 1 KΩ
(SELECT) (VO)

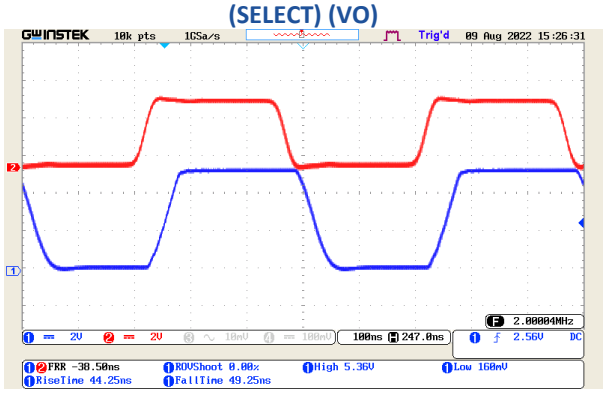


Output Overdriven Recovery, 0 V to 3 V, FAST_EN = 1
RS = 22 Ω, CL = 50 pF, RL = 1 KΩ
(SELECT) (VO)

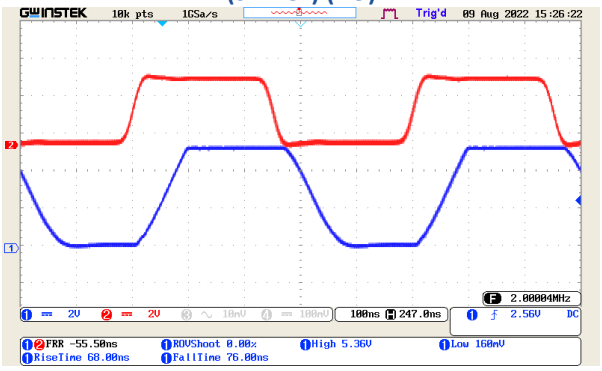
Output Overdriven Recovery, 3 V to 6 V, FAST_EN = 1
RS = 22 Ω, CL = 50 pF, RL = 1 KΩ
(SELECT) (VO)

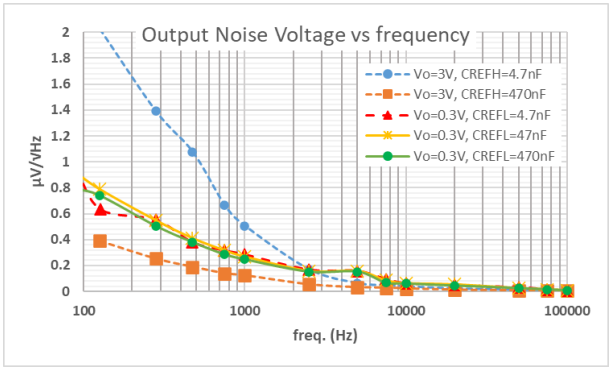


Large signal
0.3 V to 5.5 V Step @ VDD_ANA=6 V, VDD_DIG = +3.3 V
FAST_EN = 1
RS = 22 Ω, CL = 330 pF, RL = 1 KΩ
(SELECT) (VO)

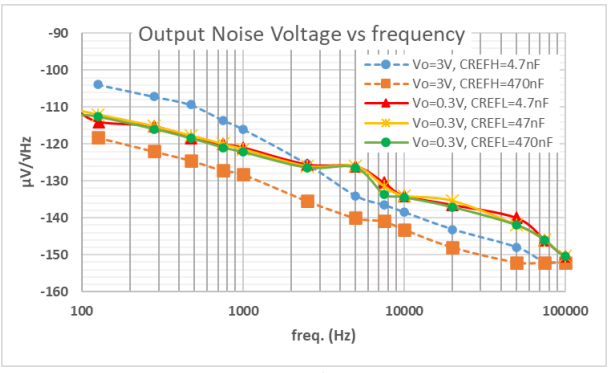


Large signal
0.3 V to 5.5 V Step @ VDD_ANA=6 V, VDD_DIG = +3.3 V
FAST_EN = 0
RS = 22 Ω, CL = 330 pF, RL = 1 KΩ
(SELECT) (VO)



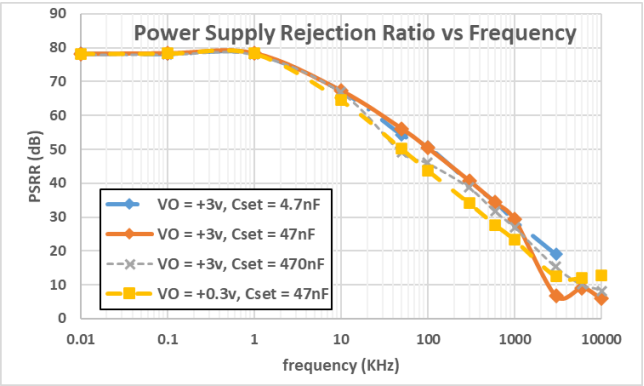


Noise uv/sqrt(Hz)

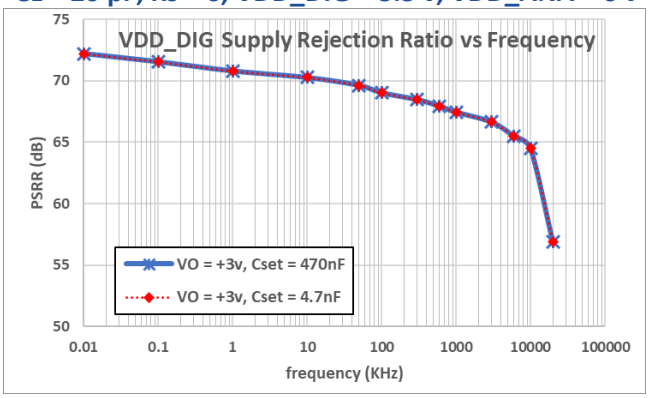


Noise dbm/sqrt(Hz)

CL = 20 pF, Rs = 0, VDD_DIG = 3.3 v, VDD_ANA = 6 v



CL = 20 pF, Rs = 0, VDD_DIG = 3.3 v, VDD_ANA = 6 v



Pin Functions

GND: Ground. Tie these pads to local ground plate on PCB. To ensure proper electrical and Thermal performance connect all pins with wide polygon to ground.

VDD_ANA: The VDD_ANA pin supplies current to the ASPGC4X20's internal Output Buffer and to the internal Reference block. This pin must be locally bypassed with an external, low ESR capacitor of at least 4.7µF. The VDD_ANA pin voltage level is positive and should be set between +3V to +12V for best chip performance.

VDD_DIG: The VDD_DIG pin supplies current to the ASPGC4X20's internal SELECT input section and to the internal monitoring block. This pin must be locally bypassed with an external, low ESR capacitor of at least 1µF. The VDD_DIG pin voltage level is positive and should be set between 2.5V to 5V for best chip performance.

$REFL_{MON}$, $REFH_{MON}$: ASPGC4X20 Monitoring Reference pads. For R_{REF1V} equal to 10Kohm, a fixed current of 101µA flows out from these pins through a single external resistor (R_{HMON}, R_{LMON}) connected between ground and each pad, which sets a positive voltage on each pad to program the monitoring reference levels. For correct function of monitoring block, the value of R_{HMON} must SELECTed greater than R_{LMON} ($REFL_{MON}$ pin voltage must be lower than $REFH_{MON}$). In order to reject high frequency noise a parallel capacitor (C_{HMON} and C_{LMON}) can be used with R_{HMON} and R_{LMON}. Do not use more than 10nF for C_{HMON} and C_{LMON}.

REFL, REFH: ASPGC4X20 Output voltage levels Reference pads. For R_{REF1V} equal to 10Kohm, a fixed current of 101µA flows out from these pins through a single external resistor (R_{REFH}, R_{REFL}) connected between ground and each pad, which sets a positive voltage on each pad to program the output voltage reference levels. The value of R_{REFH} must be selected greater than R_{REFL} (REFL pin voltage must be lower than REFH). In order to reject high frequency noise a parallel capacitor (CREFH and CREFL) can be used with RHMON and RLMON. Do not use more than 1µF for CREFH and CREFL.

REF1V: Current Reference pad. A 1.01V is internally applied between this pad and GND. Connect a 1% 10K resistor between this pad and GND to set a 101uA reference current that flows out from REFL, REFH, $REFH_{MON}$ and $REFL_{MON}$ pads.

$FAULT_{RSTX}$: Monitoring digital output flag. The pad output High level voltage is VDD_DIG and Low level voltage is 0V. The pin output level is High if MON_{INX} voltage is between $REFL_{MON}$ and $REFH_{MON}$ and is Low otherwise. High to low transition of this pad happens immediately (300ns delay) and at MON_{INX} <$REFL_{MON}$ or >$REFH_{MON}$ and low to high transition happens with a typical 82ms delay after

$REFLMON+25mV < MON_{INX} < REFH_{MON}-25mV$

MON_{INX}: Monitoring input. This pad should be connected in remote sense condition (without current) to a negative voltage relative to ground. The function of monitoring is explained above. Two protection diode is internally connected between this pad and VDD_ANA/GND pads so the applied voltage on MONINX pad must be between VDD_ANA and GND.

VO_X: ASPGC4X20 output pad. This pad is internally driven by a unity gain amplifier with 60MHz bandwidth, a 70V/us (Up to 120V/us by FST_EN) slew rate and a 70deg phase margin at 20pF capacitive load. The maximum output capacitive load is 30pF for stability. For more capacitive loads connect a 22Ω series resistor (RS) in the output. The output current limit is 23mA DC (up to 45mA with FST_EN) and 500mA peak (less than 200ns). This pad voltage levels is set by REFH and REFL pads. The $VO_x = V_{REFL}$ if SELECT=Low and $VO_X=V_{REFH}$ if SELECT=High.

SELECT: ASPGC4X20 digital input. The pad input High level voltage is VDD_DIG and Low level is 0V. This pad sets VO_X voltage level on REFH and REFL voltage. The $VO_x = V_{REFL}$ if SELECT=Low and $VO_X=V_{REFH}$ if SELECT=High. SELECT pad is

internally protected for input voltages above VDD_DIG and below 0V. Minimum input pulse width is 60ns. This pad is internally pulled down.

FST_EN: Fast operation mode enable pad. In fast operation mode the supply current of the ASPGC4X20 increases to about 2 time more than typical usage continually so the outputs slew rate and bandwidth increases to 120V/us and 90MHz respectively. The current usage is doubled in Fast mode. Fast mode operation is recommended if extra power consumption is ignorable in the system. This pad is internally pulled down.

THERMAL_FLAG: Over temperature output digital flag pad. The pad output Low and High voltage levels are 0V and VDD_DIG, respectively. The output is LOW when the temperature is below 180^{o}C and is high otherwise.

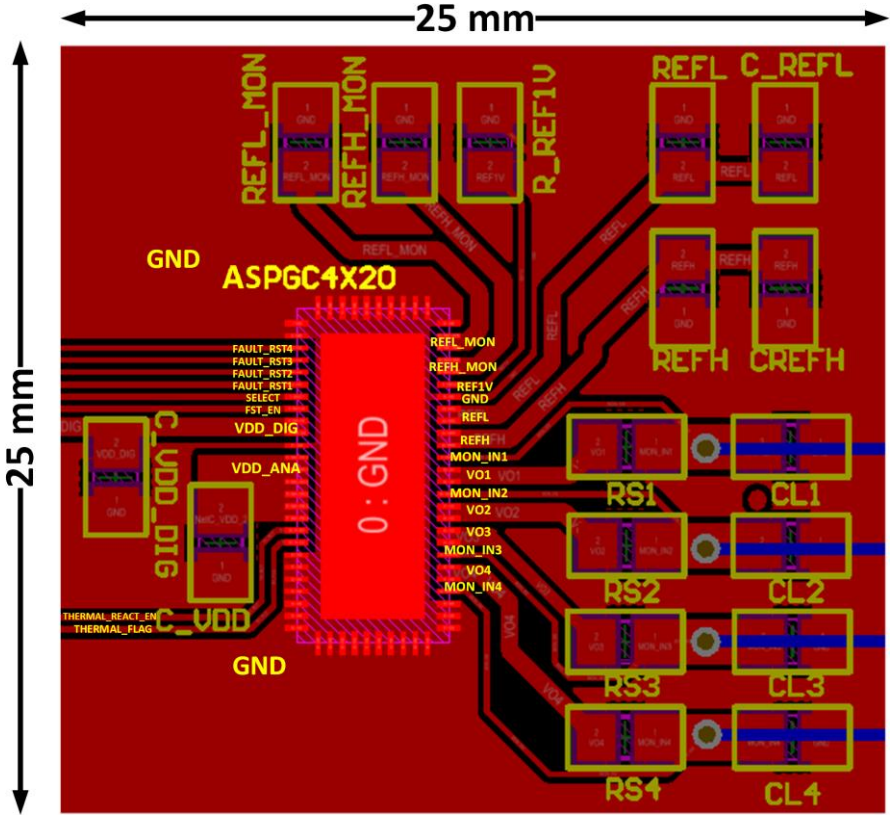
THERMAL_REACT_EN: Over temperature (OT) reaction enable pad. This pad is a pulled up digital input. Tie it to GND to disable the OT reaction mode and leave it to enable that. In OT reaction mode the supply current usage and outputs current limit level is decrease by 80% while the chip internal temperature is increased above 180^{o}C.

Application Information

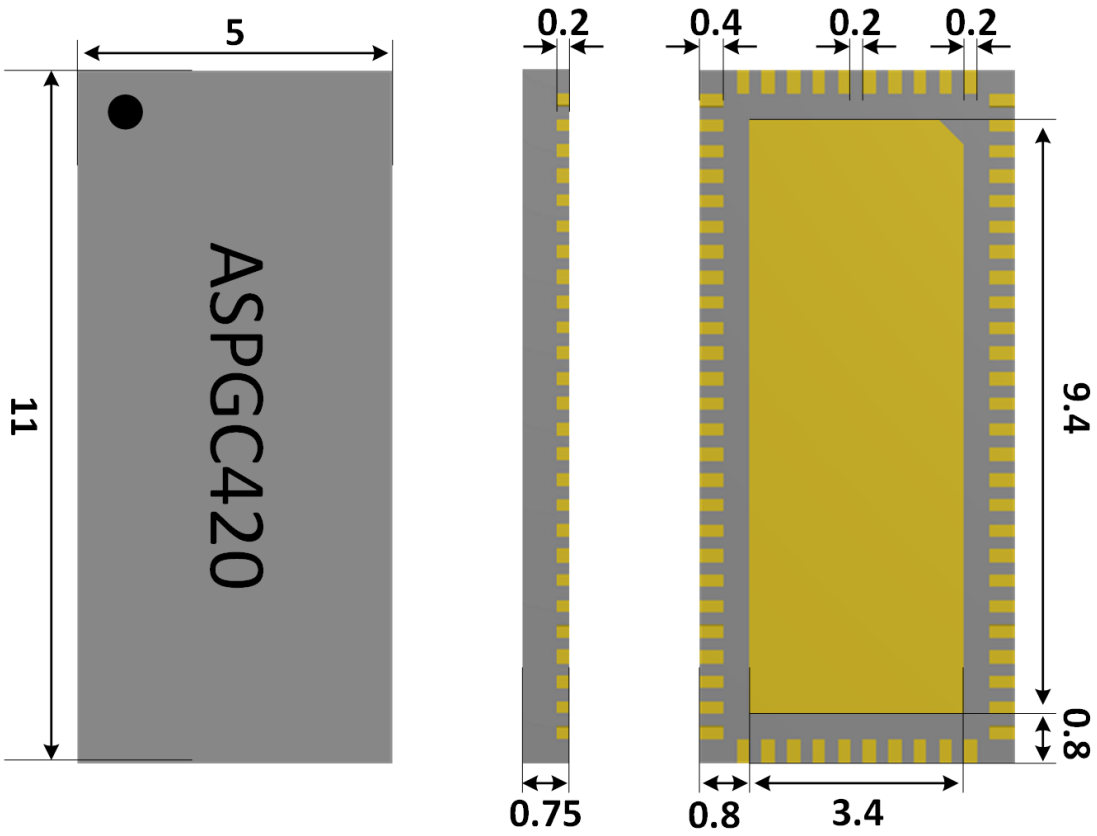
PCB Layout

The ASPGC4X20 includes quad negative gate control and monitor. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 3 for a suggested layout. Ensure that the grounding and heat sinking are acceptable. A few rules to keep in mind are:

1. Place the R_{REFL}, R_{REFH}, $R_{REFHMON}$, $R_{REFLMON}$ and R_{REF1V} resistors as close as possible to their respective pins.
2. Place the C_{REFH} and C_{REFL} capacitors as close as possible to their respective resistors.
3. Place the RS resistors as close as possible to their respective pins.
4. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the ASPGC4X20.
5. CL capacitors can be placed far from the ASPGC4X20 if RS resistors have been used.
6. It is recommended to connect MON_IN track without DC current path to monitor the consumer voltage level.
7. Use vias to connect the GND copper area to the board's internal ground plane. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board.



All dimensions are in mm ± 0.05 mm



72 pin QFN Package