ASP2010

40 V, 2 A EM Compliant Switching Regulator with 2-Output Configurable LDO

Features

- **Step-Down Switch Mode Power Supply**
- **Wide Input Voltage Range: 8V to 40V**
- **2 A Buck Output Current**
- **2V to 12.5V Output Voltage**
- **Selectable Switching Frequency: 0.2 MHz to 2.5 MHz**
- **Adjustable 10% Accurate Current Limit**
- **Configurable Output LDO Array**
  - Two 1 A Parallelable Outputs
  - Outputs Adjustable From 0 V to 12 V
  - Low Output Noise: 6µvrms (10Hz to 100kHz)
- **Programmable Soft-Start**

Applications

- Automotive Battery Regulation
- FPGA, DSP, ASIC and Microprocessor Supplies
- Servers and Storage Devices
- RF Transceivers

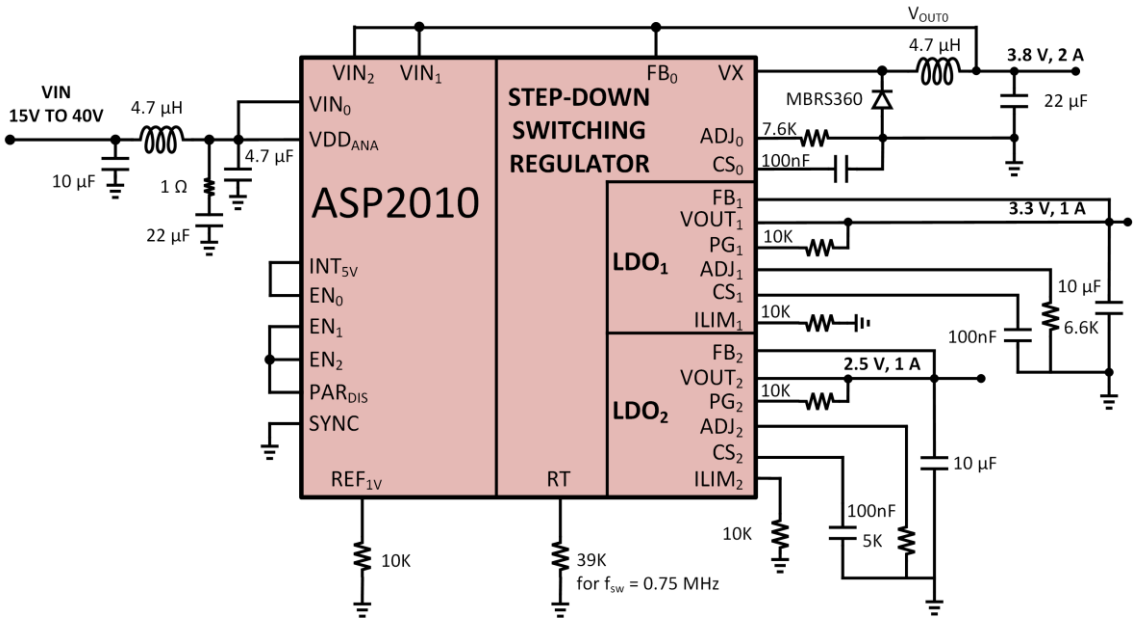
Description

The ASP2010 is a 40 V, 2 A step-down High-Side switch and regulator controller chip with a 2-output configurable LDO array. Operating over an input voltage range of 8 V to 40 V, the ASP2010 buck regulator supports an output voltage range of 2V to 12.5 V and wide selectable switching frequency range of 200 kHz to 2.5 MHz each ADJ by a single resistor. The buck regulator has synchronization possibility and generates low switching noise. Following the buck regulator is a couple of 1 A linear regulators whose outputs may be connected in parallel to accommodate a wide variety of load combinations.

The ASP2010 is packaged in thermally enhanced QFN package and has high efficiency which makes it a good solution for high density power management units.

Typical Application

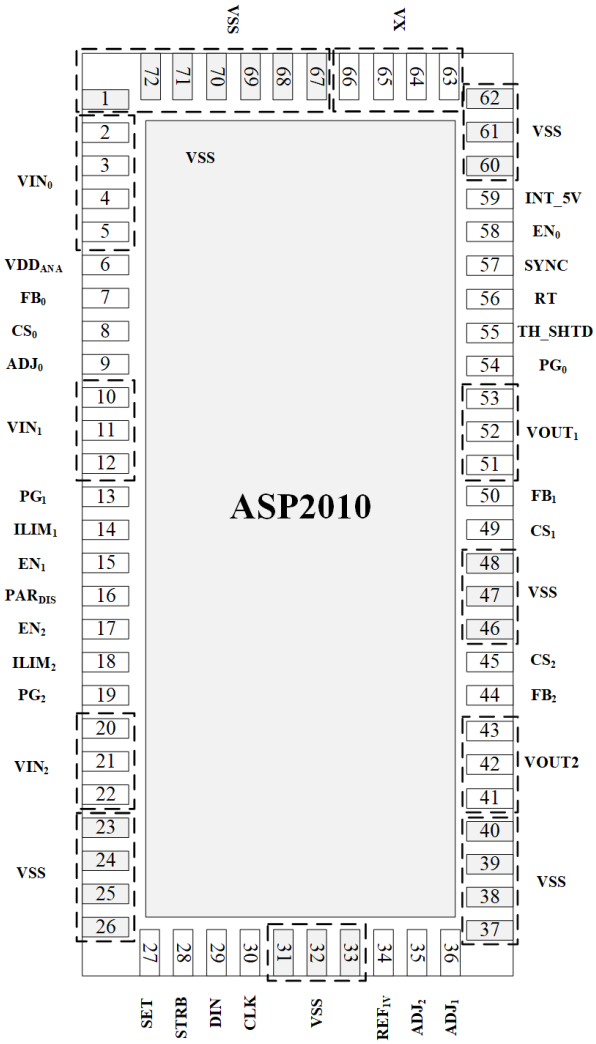
Dual 1A Regulated Outputs



Absolute Maximum Rating

VIN_0, VDD_{ANA}, VX ..... 45 V
EN_0, INT_5V, EN_1, EN_2, PAR_{DIS}, TH_SHTD ..... 5.5 V
SYNC, RT, ADJ_0, ADJ_1, ADJ_2, REF_{1V} ..... 5.5 V
PG_0, PG_1, PG_2, $ILIM_1$, $ILIM_2$, FB_0, CS_0 ..... 5.5 V
SET, STRB, DIN, CLK..... 5.5V
VIN_1, VIN_2 ..... 13 V
FB_1, FB_2, CS_1, CS_2 .....13 V
$VOUT_1$, $VOUT_2$ ..... 13 V
Maximum Junction Temperature..... 200 °C

Pin Configuration

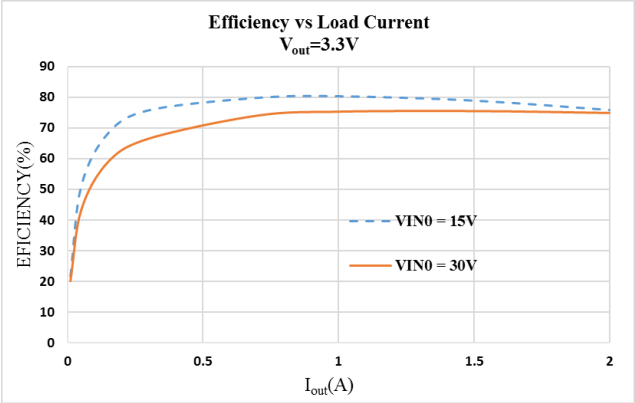


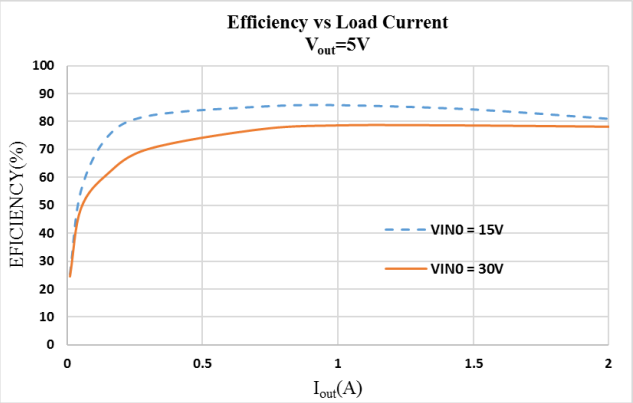
Electrical Characteristics

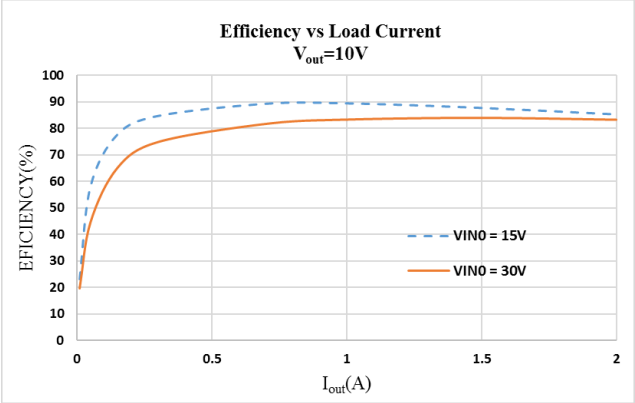
Parameter	Conditions	MIN	TYP	MAX	UNITS
Buck Regulator					
Minimum Required VIN_0 Input Voltage to run	VOUT = 5V	7.4		8.5	V
$VOUT_0$ DC Voltage	0 A < I_{out} < 2 A ADJ_0 = 4 kΩ 0 A < I_{out} < 2 A ADJ_0 = 24 kΩ		2 12		V V
Quiescent Current into VIN_0	EN_0, EN_1, EN_2 = 0		5		mA
$VOUT_0$ Line Regulation	8V < VIN_0 < 40V, I_{out} = 2 A		±0.5		%
$VOUT_0$ Load Regulation	VIN_0 = 28 V, 0 A < I_{out} < 2 A		±1		%
$VOUT_0$ RMS Voltage Ripple	VIN_0= 28 V, $VOUT_0$ = 5 V, 0 A < I_{out} <2 A		7.4		mV
$VOUT_0$ RMS Output Noise	$VOUT_0$ = 5 V, I_{Load} = 1 A, CS_0 = 10 nF 10Hz to 100 kHz		198		µV
$VOUT_0$ RMS Output Noise	$VOUT_0$ = 5 V, I_{Load} = 1 A, CS_0 = 470 nF 10Hz to 100 kHz		140		µV
Switching Frequency	RT = 28 kΩ RT = 160 kΩ		1000 200		kHz kHz
EN_0 Threshold Voltage	OFF			0.5	V
EN_0 Threshold Voltage	ON	1			V
ADJ_0 Pin Current	R_{ref} = 10 kΩ	98	100	102	µA
RT Pin Voltage		0.99	1.01	1.03	V
SYNC Input Low Threshold				0.5	V
SYNC Input High Threshold		1			V
LDO Array					
ADJ_1, ADJ_2 Pin Current	R_{ref} = 10 kΩ	98	100	102	µA
REF1V Pin Voltage		0.99	1.01	1.03	V
LDO1, LDO2 Dropout Voltage	I_{Load} = 100 mA I_{Load} = 700 mA			0.09 0.2	V V
LDO1, LDO2 Maximum Dropout Voltage	R_{LIM} = 19k, I_{Load} = 390 mA R_{LIM} = 19k, I_{Load} = 600 mA R_{LIM} = 19k, I_{Load} = 800 mA			9.5 8 6.5	V V V
$VOUT_1$, $VOUT_2$ RMS Output Noise	$VOUT_{1,2}$ = 5 V, I_{Load} = 400 mA, 100 Hz to 100 kHz, $CS_{1,2}$ = 47 nF		29		µV
$VOUT_1$, $VOUT_2$ RMS Output Noise	$VOUT_{1,2}$ = 5 V, I_{Load} = 400 mA, 100 Hz to 100 kHz, $CS_{1,2}$ = 470 nF		6		µV
$EN_{1,2}$ Threshold Voltage	OFF			0.5	V
$EN_{1,2}$ Threshold Voltage	ON	1			V

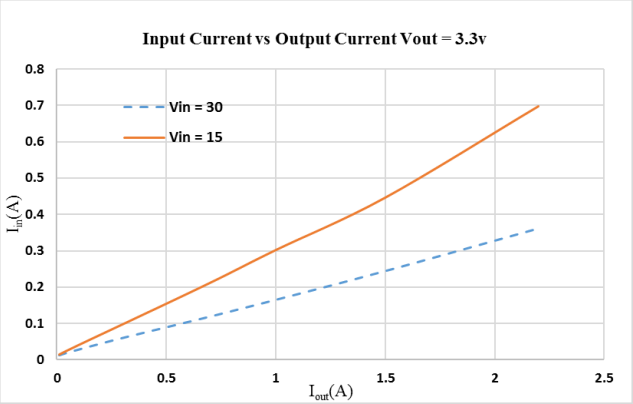
DC/DC conv. Typical Performance Characteristics

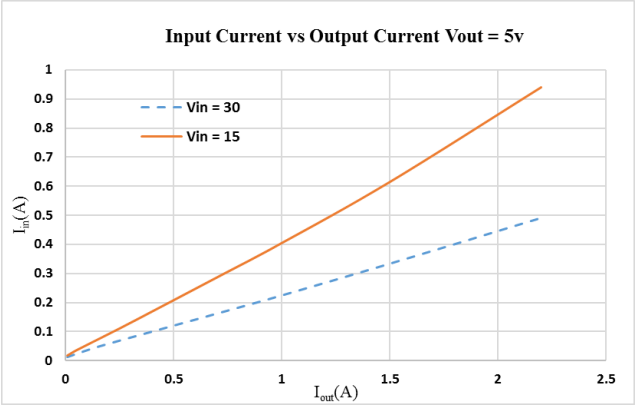
TA = 25◦ unless otherwise noted

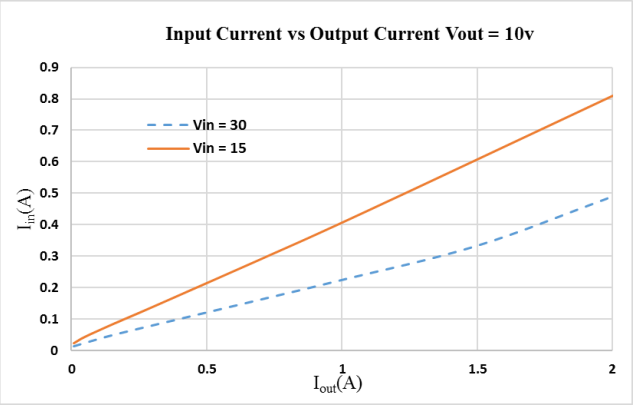












DC/DC conv. Typical Performance Characteristics

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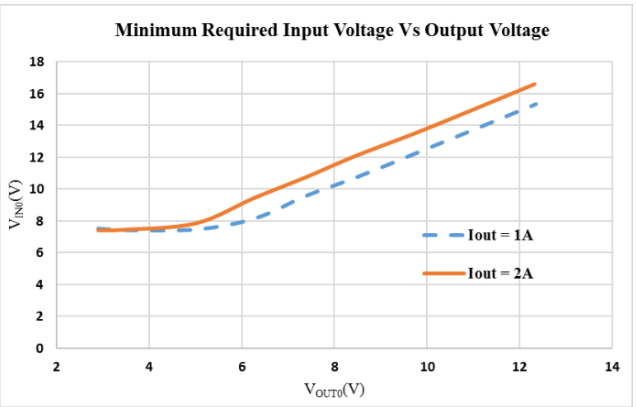
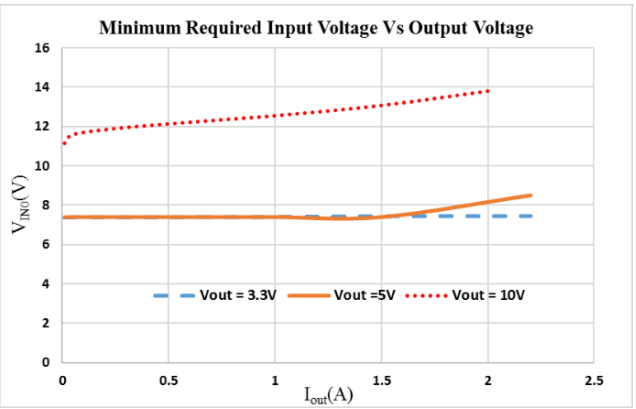
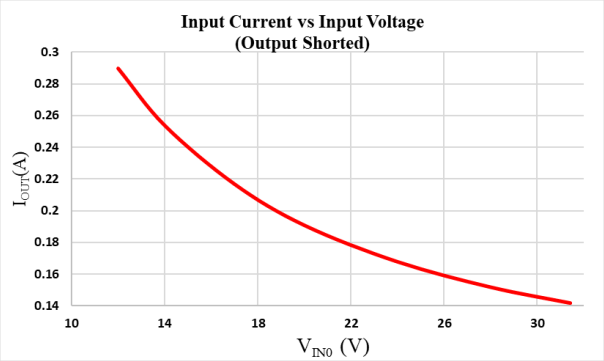
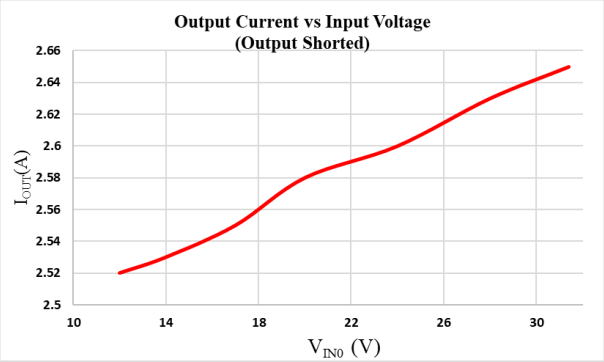


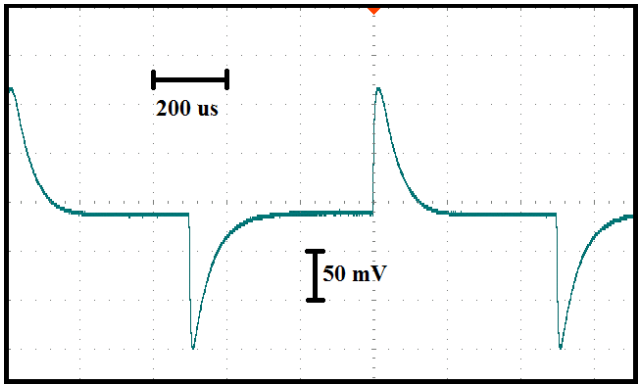




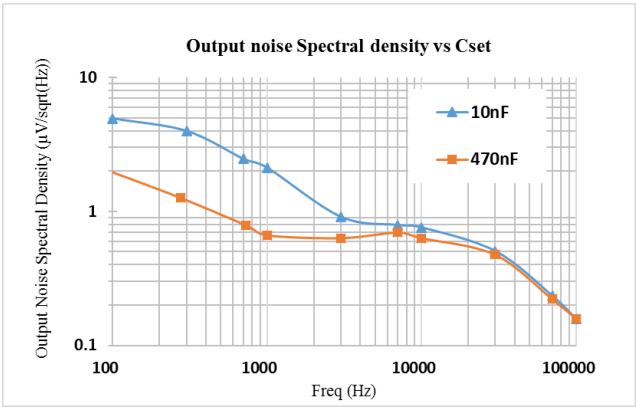


Load Transient Response

$IOUT_0$ = 200 mA ~ 800 mA



$VOUT_0$ = 5 V, C_{OUT-BK} = 22 µF



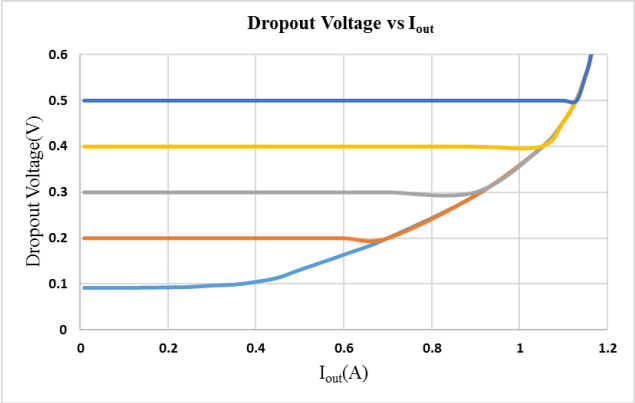
VIN_0 = 30 V

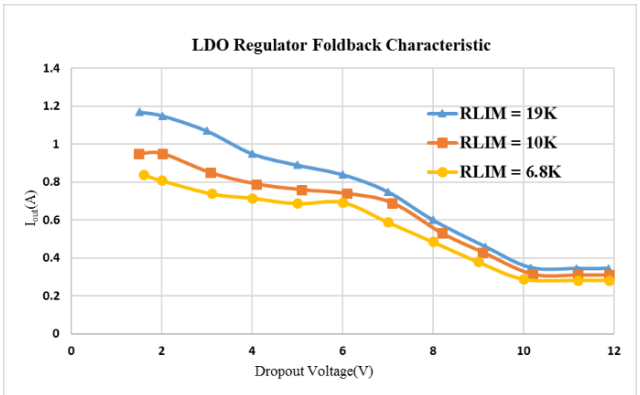
$VOUT_0$ = 5.5 V, C_{OUT-BK} = 22 µF

I_{OUT0} = 1 A, f_S = 750 kHz

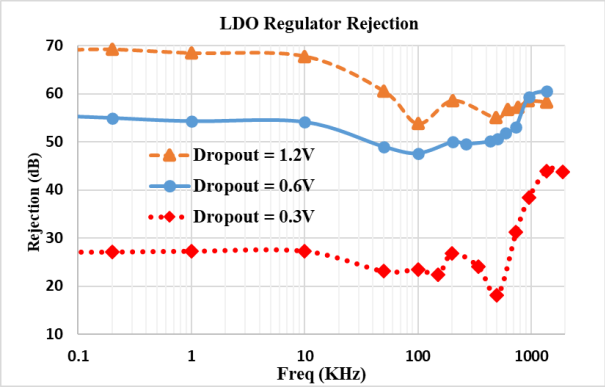
LDO Typical Performance Characteristics

TA = 25◦ unless otherwise noted

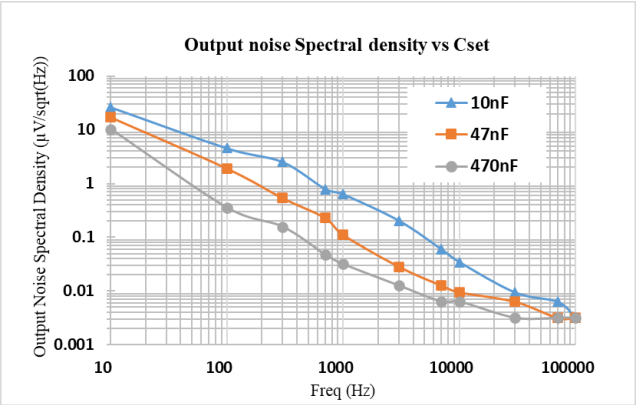




RLIM is ILIM resistor to VSS

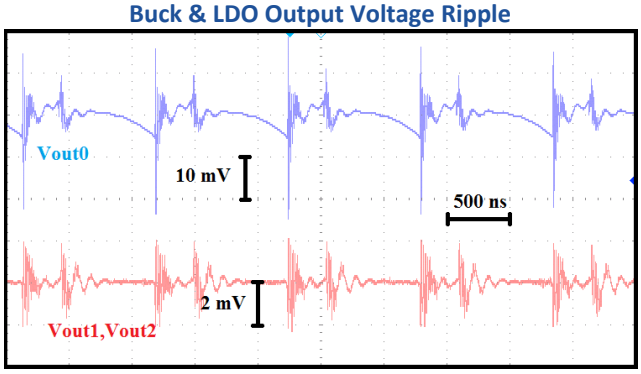


IOUT1,2 = 600 mA



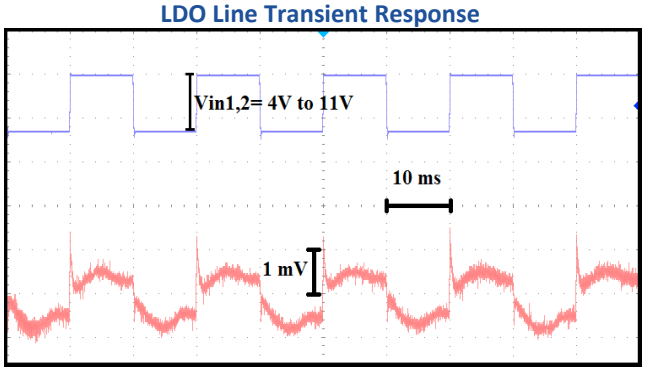
VOUT0 = 5.6 V
VOUT1,2 = 5 V, COUT-LDO =10 µF
IOUT1,2 = 1 A

Buck & LDO Output Voltage Ripple



VIN0 = 30 V
VOUT0 = 5 V, COUT-BK = 22 µF
VOUT1,2 = 4 V, COUT-LDO =10 µF
IOUT1 = IOUT2 = 400 mA (Buck loaded with LDO)

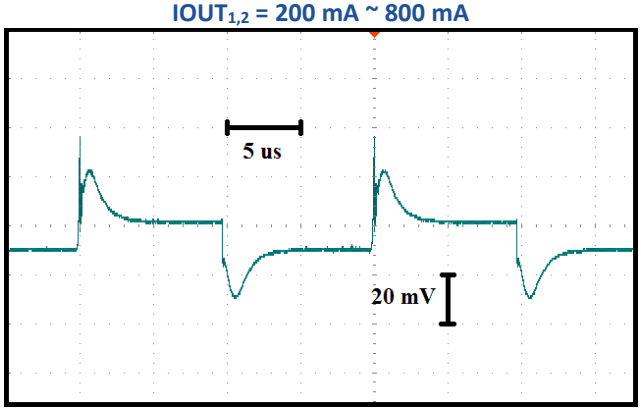
LDO Line Transient Response



VOUT1,2 = 3.3 V, COUT-LDO = 10 µF
IOUT1 = IOUT2 = 400 mA (Buck loaded with LDO)

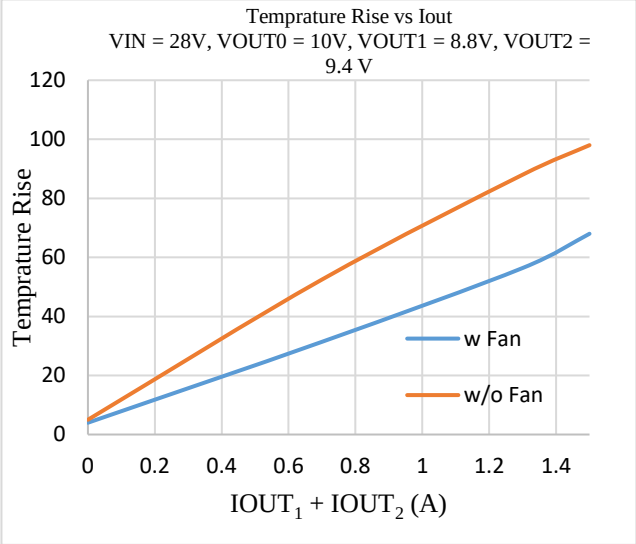
Load Transient Response

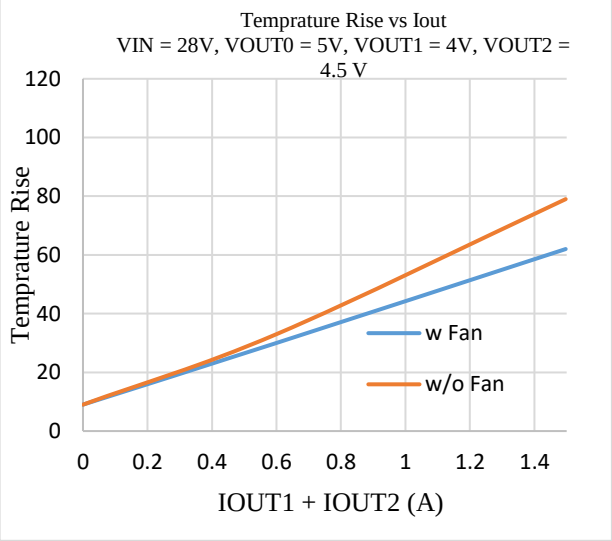
$IOUT_{1,2}$ = 200 mA ~ 800 mA



$VOUT_0$ = 5 V, C_{OUT-BK} = 22 µF

$VOUT_{1,2}$ = 4 V, $C_{OUT-LDO}$ = 10 µF





Pin Functions

VSS: Ground. Tie these pads to local ground plate on PCB. To ensure proper electrical and Thermal performance connect all pins with wide polygon to ground.

VIN_0: The VIN_0 pin supplies current to the ASP2010's internal regulator and to the internal power switch. This pin must be locally bypassed with an external, low ESR capacitor of at least 4.7 µF. It's recommended to use low EMI filter before VIN_0 pin as mentioned in application information.

VX: DC/DC converter High-side switch drain. This pad should connect to converter Output filter inductor and the Diode Cathode pin in a structure with low electromagnetic emission (refer to PCB Layout recommendation section).

FB_0, FB_1, FB_2: Regulator VOUT feedback. Connect these pads to regulator output node, which want to be regulated. To have a well-regulated voltage use a remote sense connection of this pad to output node. Avoid to near switching tracks to feedback track.

PG_0, PG_1, PG_2: Power-Good Flag. The PG_X pin is an open-drain logic pin connected to the output of the power good comparator. PG asserts low if output voltage is less than 90% of desired voltage and if output voltage is greater than 90% desired voltage the PG pin de-asserts and becomes high impedance with 24 µs delay. The PG pin may be pulled to 5V or less using a 10 kΩ or more resistor. In LDO regulators fast start ends after PG flag becomes high impedance.

REF_{1V}: Reference 1 V pad. This pin has a 1 V fixed reference voltage, which makes 100 µA fixed current on the 10 kΩ external connected resistor. This current is mirrored in the chip to generate ADJ_0, ADJ_1 and ADJ_2 pins current. If another value is used for REF_{1V} resistor ADJ0, ADJ1 and ADJ2 pins current will be

$$I_{ADJ} = \frac{1\ V}{R_{REF1v}}$$

And regulators' output voltage should be calculated based on this current. Do not connect less than 5 kΩ resistor to this pin.

ADJ_0, ADJ_1, and ADJ2: These pins Adjusts the regulation point for each regulator. For $RREF_{1V}$ equal to 10 kΩ, a fixed current of 100 µA flows out of these pins through a single external resistor (R_{ADJ0}, R_{ADJ1}, R_{ADJ2}), which programs the output voltage of each regulator. Output voltage range is from 2V to 12.5V for buck regulator and 0 V to 12 V for LDOs. The required resistor from the formula:

$$R_{ADJ} = V_{OUT} \times 2000\ \Omega$$

CS_0, CS_1, and CS2: These pads control the regulators output voltage soft start speed and output noise spectrum, using a capacitor. LDO regulators have fast start ability. During startup operation and before PG flag become high impedance, a 1 mA current flows out of CS_1 and CS_2 pins and fastens linear regulators output voltage rise speed. Soft start duration is a function of CS capacitor:

$$T_{SOFT-START(BUCK)} = 4 \times 13.2k \times C_{SET0}$$

$$T_{FAST-START(LDO)} = 0.5 \times C_{SET1,2} \times R_{ADJ1,2}$$

$ILIM_1$,$ILIM_2$: External Current Limit Programming. This pin externally programs current limit with following function relative to R_{LIM} (kΩ) resistor connected from this pin to ground:

$$I_{LIM} = 0.8\frac{R_{LIM}}{5.3 + R_{LIM}} + 0.4\ (A)$$

EN_0, EN_1, EN_2: Regulator Enable pin. Each of switching or LDO regulators are enable if relative EN pin voltage level is more than 1 V or disable if voltage level is less than 0.5 V. These pins are internally pull down with 100 kΩ resistor.

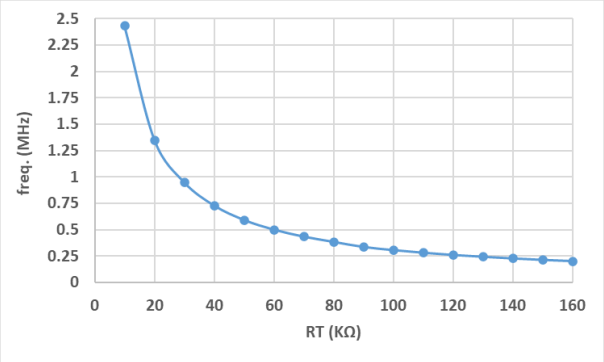
INT_5V: This pin is connected to the internal 5 V regulator of the chip with a 2 kΩ resistor. It can be used to normal enable the buck converter by connecting the EN_0 pin to INT_5V.

PAR_{DIS}: LDO Regulator Parallel Disable. This pin externally controls LDO regulators to be in parallel state or independent. Tie this pin to ground to parallel LDO regulators and leave floating for independent operation. PAR_{DIS} pin is internally pull up. To parallel two LDO regulators refer to Applications information.

SYNC: This is the external clock synchronization input. Tie to a clock source for synchronization. Clock edges rise time and fall time should be faster than 1µs. The internal oscillator of the ASP2010 can be synchronized by applying an external 250 kHz to 2 MHz clock to the SYNC pin. The resistor tied from the RT pin to ground should be chosen such that the ASP2010 oscillates 20% lower than the intended synchronization frequency. Do not leave this pin floating.

RT: The RT pin is used to program the switching frequency of the ASP2010 by connecting a resistor from this pin to ground.

RT (kΩ)	Freq. (kHz)
12	2000
22.5	1500
28	1000
39	750
82	375
125	250



$VOUT_1$, $VOUT_2$: LDO Output. These pins supply power to the load. Connect $VOUT_1$ and $VOUT_2$ pins together In Parallel Mode. Stability requirements demand 10 µF ceramic output capacitor with an ESR less than 100 mΩ to prevent oscillations.

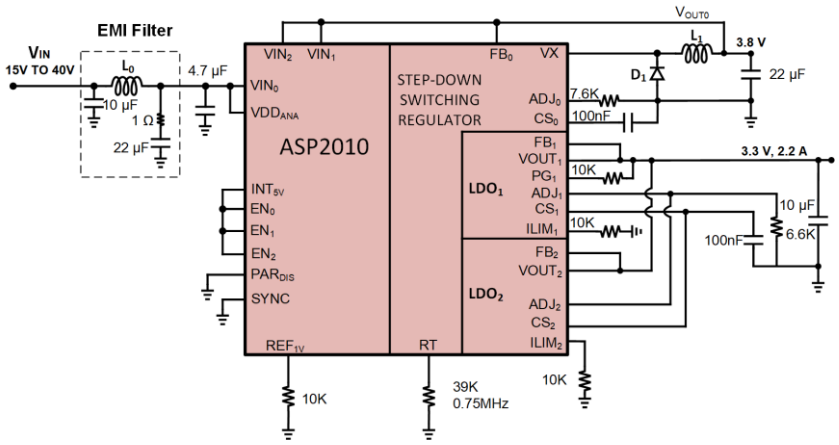
TH_SHDN: Thermal shutdown flag. This pin generates the 5 V thermal shutdown signal when the chip temperature reaches 185 °C. in addition, TH_SHDN flag disables all regulators and enables them again when the chip temperature decreases to 165 °C. this pin can be tied to VSS if user does not need thermal shutdown reaction.

SET, STRB, DIN, CLK: These pins are used for productions tests. Tie these pins to VSS.

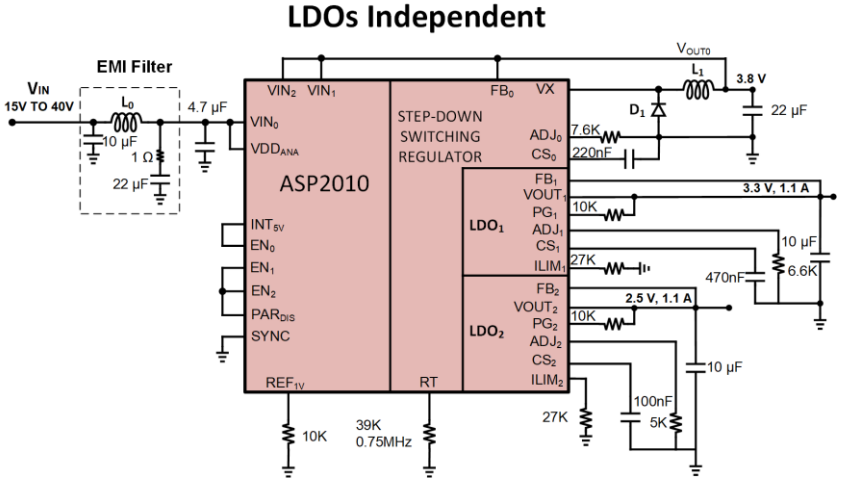
VIN_0	$VOUT_0$	C_{OUT}	R_{ADJ0} (kΩ)	f_{opt} (kHz)	RT_{opt} (kΩ)	f_{MAX} (kHz)	RT_{MIN} (KΩ)
8V ~ 35V	1.50V	22μF 1206	3	400	50	700	43
8V ~ 35V	2.5V	22μF 1206	5	600	75	900	33
8V ~ 15V	3.5V	22μF 1206	7	850	35	100	33
15V ~ 35V	3.5V	22μF 1206	7	750	40	900	30
8V ~ 35V	4.5V	22μF 1206	9	850	35	1000	30
8V ~ 20V	5.5	22μF 1206	11	1000	30	1200	25
20V ~ 35V	5.5	22μF 1206	11	900	33	1100	27
8V ~ 15V	6.5	22μF 1206	13	950	32	1200	25
15V ~ 35V	6.5	22μF 1206	13	850	35	1000	30
10V ~ 15V	7.5	22μF 1206	15	1000	30	1200	25
15V ~ 35V	7.5	22μF 1206	15	850	35	1100	27
12V ~ 20V	8.5	22μF 1206	17	1100	27	1200	25
20V ~ 35V	8.5	22μF 1206	17	900	33	1100	27
12V ~ 20V	10	22μF 1206	20	1200	25	1200	25
20V ~ 35V	10	22μF 1206	20	950	32	1100	27

Typical Applications

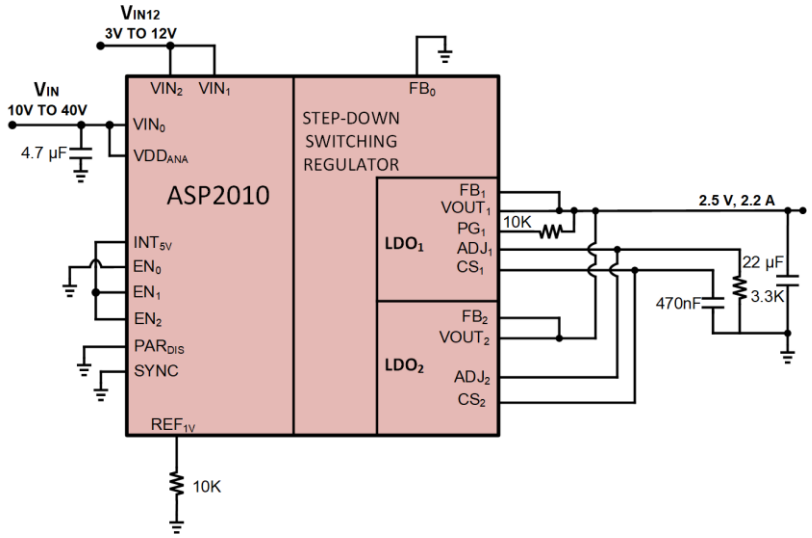
LDOs Parallel



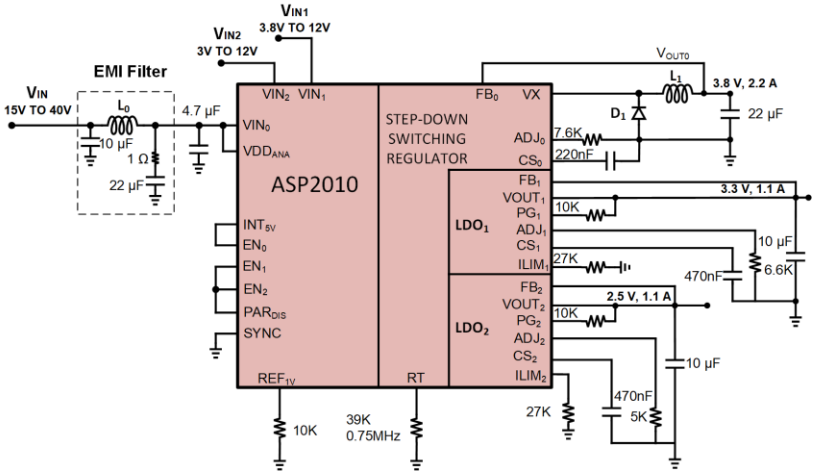
LDOs Independent



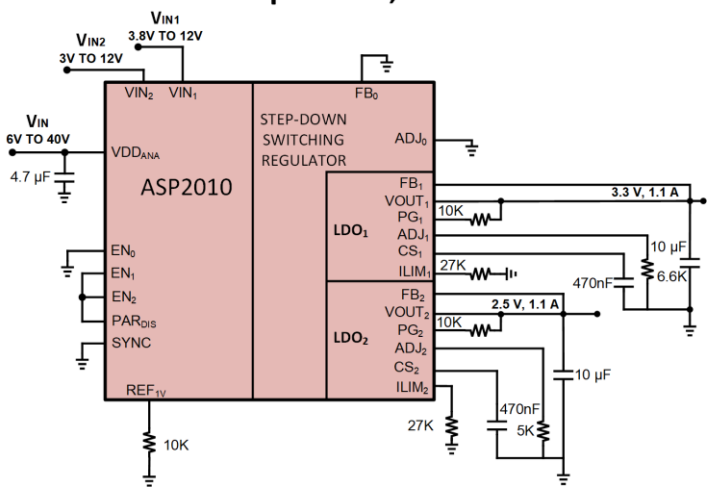
LDOs Parallel, Buck Disable



LDOs Independent, Not Connected to Buck



LDOs Independent, Buck Disable

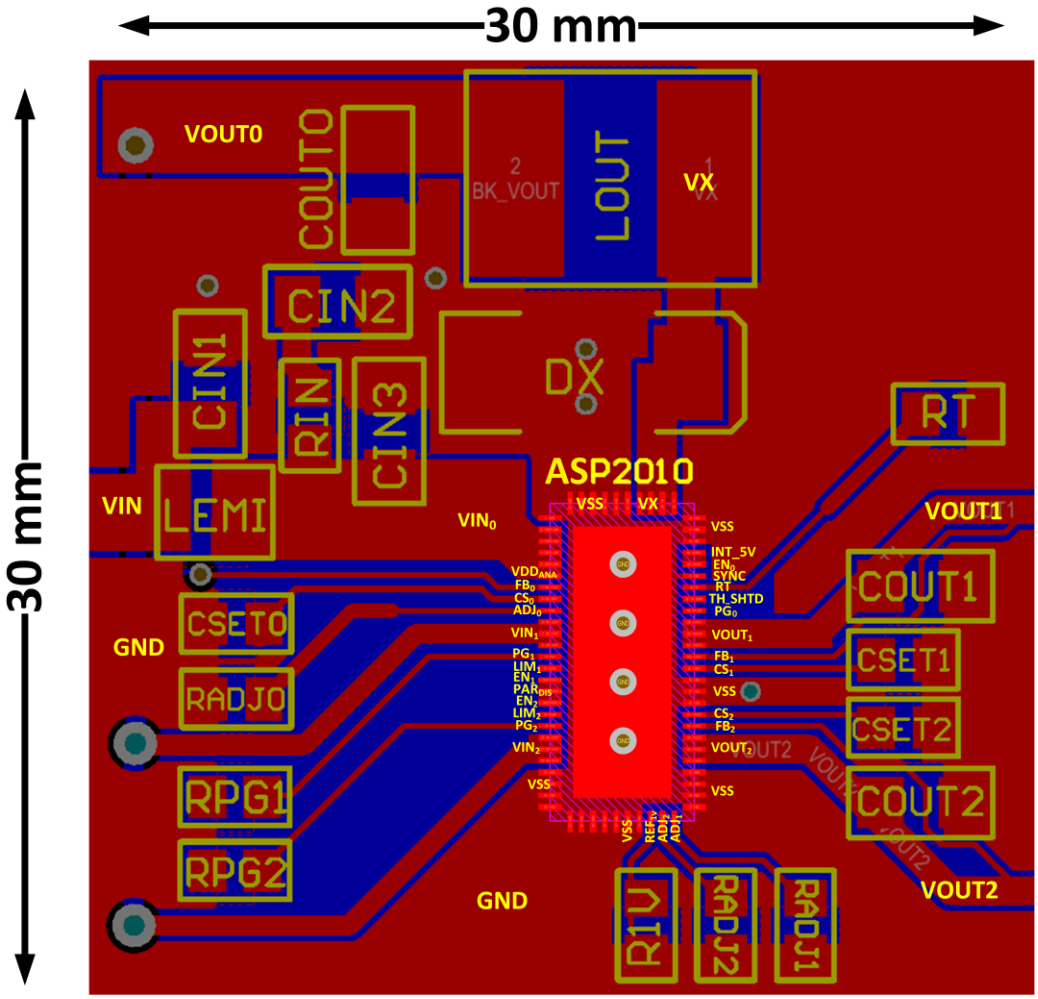


Application Information

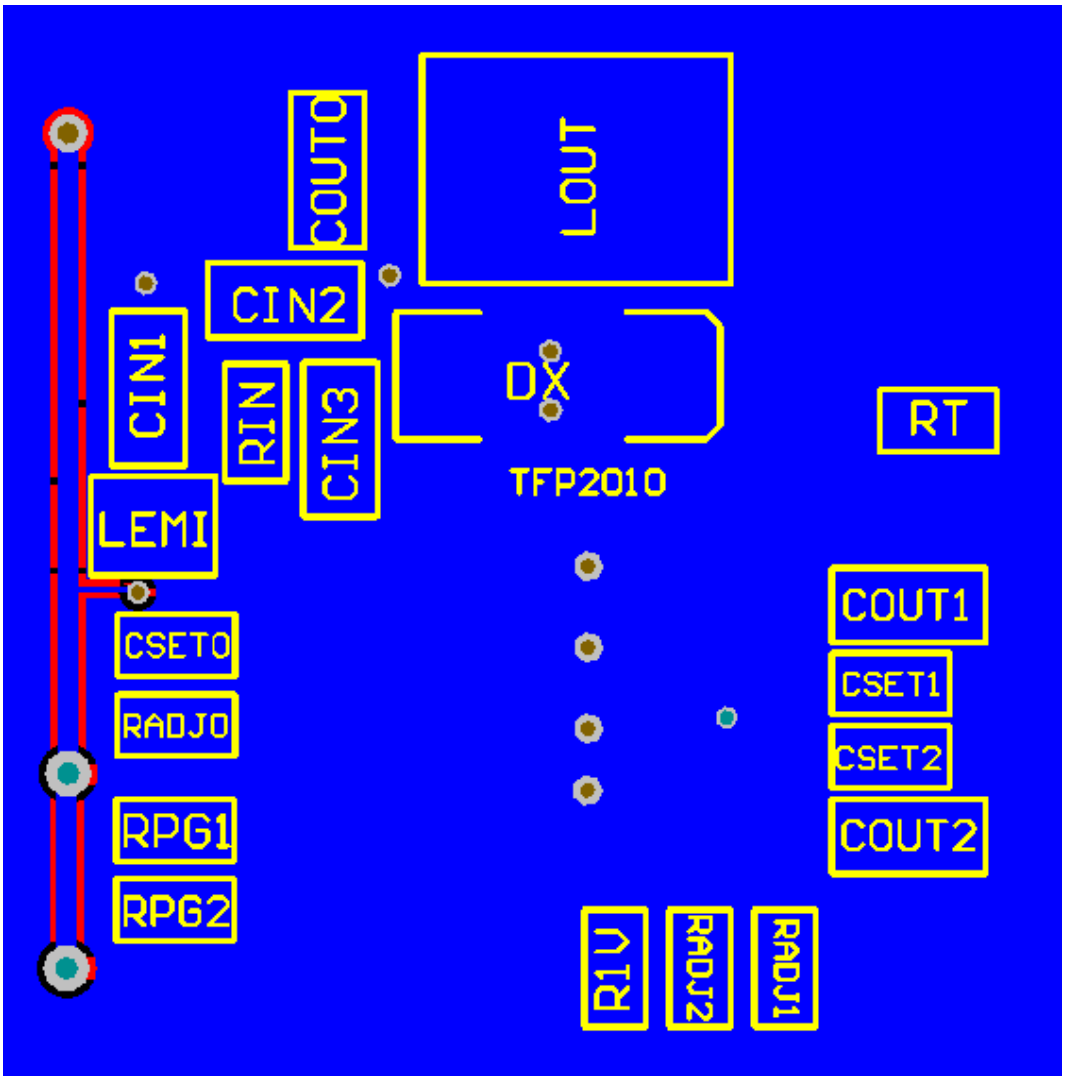
PCB Layout

The ASP2010 includes a switching power supply and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 3 for a suggested layout. Ensure that the grounding and heat sinking are acceptable. A few rules to keep in mind are:

1. Place the R_{ADJ} and RT resistors as close as possible to their respective pins.
2. Place the C_{IN} capacitor as close as possible to the VIN and GND connection of the ASP2010.
3. Place C_{OUT} capacitors as close as possible to relative VOUT and GND connection of the ASP2010.
4. Place the C_{IN} and C_{OUT} capacitors such that their ground currents flow directly adjacent or underneath the ASP2010.
5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the ASP2010.
6. Use vias to connect the GND copper area to the board's internal ground plane. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board.

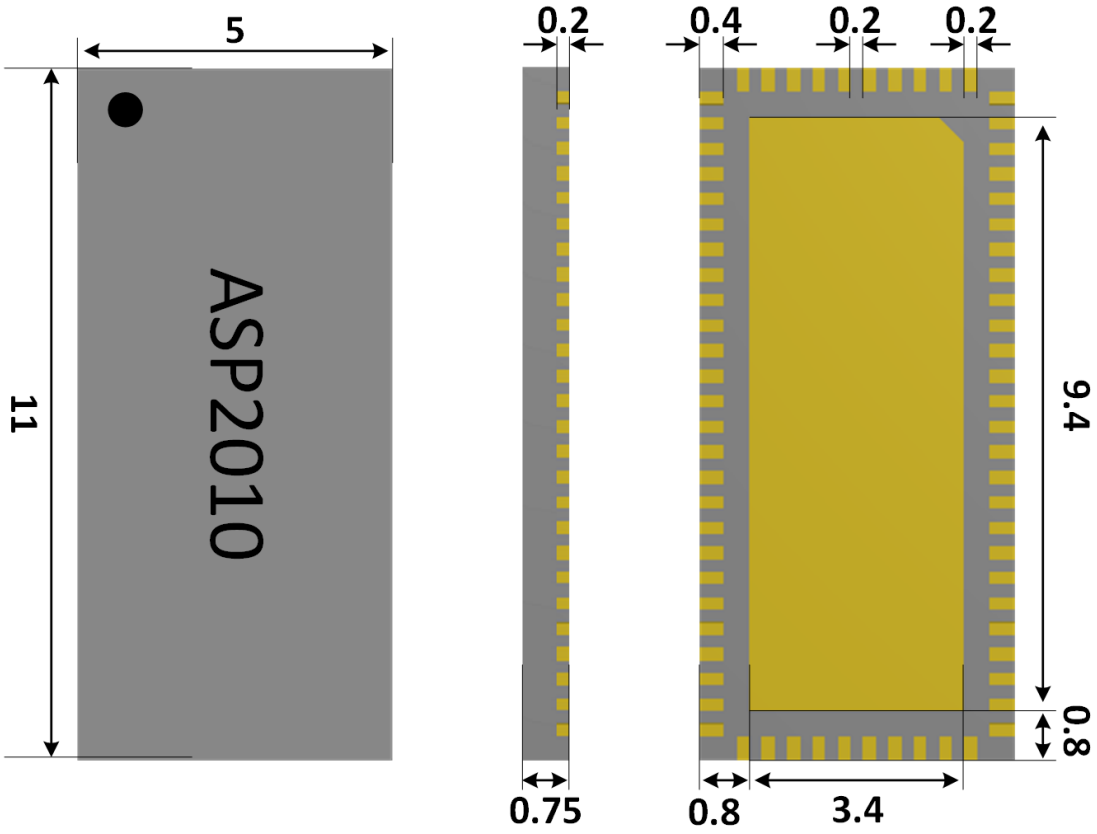


Top View


LOUT
COUT0
CIN2
CIN1
RIN
CIN3
DX
TFP2010
RT
LEMI
COUT1
CSET0
CSET1
RADJ0
CSET2
RPG1
COUT2
RPG2
R1V
RADJ2
RADJ1

Bottom View

All dimensions are in mm ± 0.05 mm



72 pin QFN Package

Recommended Off-chip Components

Component	Value	Manufacturer	Recommended Part Number
D_1	--	ONSEMI ST	MBRS360BT3G STPS3H60-Y
L_1	4.7 µH	Coil Craft Coil Craft	XAL5030-472ME XGL6030-472ME
L_0	4.7 µH	TDK	252012ALMA4R7MTAA