# ASNGC4X20

**Quadruple, Negative Voltage Low noise, 320V/µs, Rail-to-Rail Adjustable Output RF Amplifier Gate Bias Control & Monitoring**

## Features

- **Internal Op-Amp -3dB Band-Width: 60MHz, $A_V$ = 1**
- **Slew Rate: 70V/µS (320V/µS with FST_EN)**
- **Wide Analog Supply Range: -2.5V to -12V**
- **Positive Digital Supply Range: +2V to +5V**
- **Output Current: 20mA**
- **Four Separated Output Array**
  - **Output Swings Rail-to-Rail**
  - **Output Offset Voltage, Rail-to-Rail: 5mV Max**
  - **Low Output Noise: 20µvrms (10Hz to 100kHz)**
  - **Power Supply Rejection: 75dB Typ.**
  - **Programmable Soft-Start**
  - **Operating Temperature Range: –40°C to 125°C**
  - **Low Profile (5mm x 11mm x 0.75mm) QFN Package**

## Applications

- Power Management unit
- RF Amplifier Gate Control and Monitoring
- RF Transceivers Gate Control

## Description

The ASNGC4X20 is a quad negative gate control and monitor with up to 320 V/µS output slew rate. The outputs have been driven with four unity – gain amplifier with a gain-bandwidth of 60MHz and a 20mA output current to fit the requirements of high-performance RF bias boards.

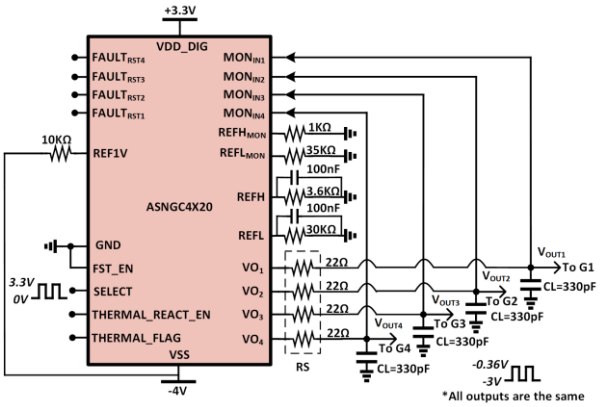
The ASNGC4X20 has a digital positive select input and quad rail to rail outputs that swing within 100mV of GND and 300mV of VSSL rail to maximize the signal dynamic range in low voltage applications.

The ASNGC4X20 has low output RMS noise and precision output voltage levels that are adjusted with only two resistors. It has four precision monitoring blocks with adjustable power good range and four output flags.

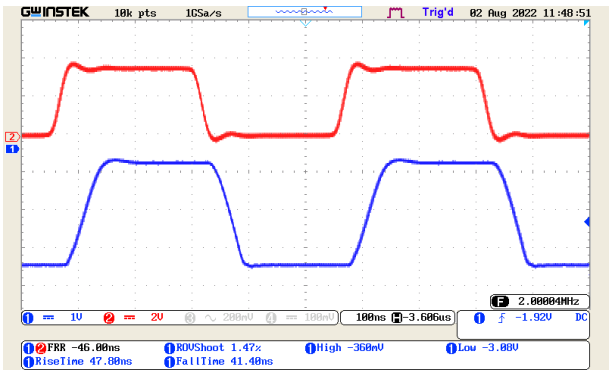
The ASNGC4X20 maintains its performance with a VSSL voltage from -3V to -12V and a VDD_DIG voltage from 2V to 5V. The Input digital select levels are GND and VDD_DIG as Low and High logical levels, respectively. The output voltage and monitoring levels can be set between VSS and GND.

# Typical Application

Quadrative Gate Control and monitoring




**Large signal**
**-0.36 V to -3 V Step @ VSS=-4.5 V, VDD_DIG = +3.3 V $FST_{EN}$ = 0**
**RS = 22 Ω, CL = 330 pF**
**(SELECT) (VO)**



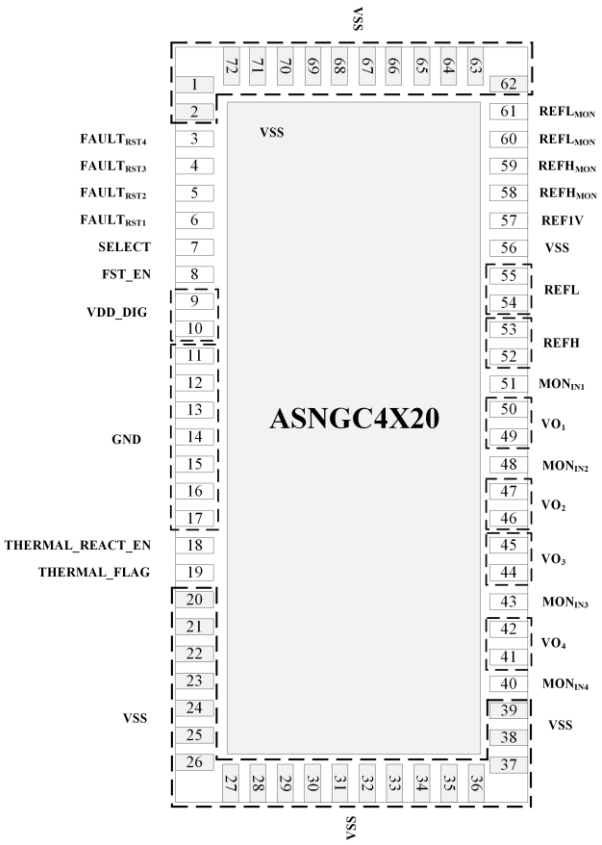
## Absolute Maximum Rating

VSSL.....+0.5 V to -13 V
VDD_DIG ..... -0.5 V to 5.5 V
VDD0..... 0 V
FAULT_RSTx..... -0.5 V to VDD_DIG +0.5 V
SELECT..... -0.5 V to VDD_DIG +0.5 V
FAST_EN..... -0.5 V to VDD_DIG +0.5 V
THERMAL_REACT_EN.....-0.5 V to VDD_DIG +0.5 V
THERMAL_FLAG.....-0.5 V to VDD_DIG +0.5 V
VOx, MON_INx..... VSSL-0.5 V to +0.5 V
REFH, REFL..... .... VSSL-0.5 V to +0.5 V
REFH_MON, REFL_MON..... VSSL-0.5 V to +0.5 V
REF1V..... VSSL-0.5 V to VSSL +5 V
Maximum Junction Temperature..... 250 °C

## Recommended Pin Voltage Range

VSSL.....-3 V to -13 V
VDD_DIG ..... 2.5 V to 5.5 V
VDD0..... 0 V
FAULT_RSTx..... Digital OUT (0 to VDD_DIG)
SELECT. ..... Digital IN (0 to VDD_DIG)
FAST_EN..... Digital IN (0 to VDD_DIG)
THERMAL_REACT_EN..... Digital IN (0 to VDD_DIG)
THERMAL_FLAG..... Digital OUT (0 to VDD_DIG)
VOx ..... VSSL+0.3 V to -0.1 V
MON_INx ..... VSSL+0.3 V to 0 V
REFH, REFL..... VSSL+0.3 V to -0.1 V
REFH_MON, REFL_MON..... VSSL+0.3 V to 0 V
REF1V..... Analog OUT (VSSL+1 V)
Maximum Junction Temperature..... 150 °C

## Pin Configuration



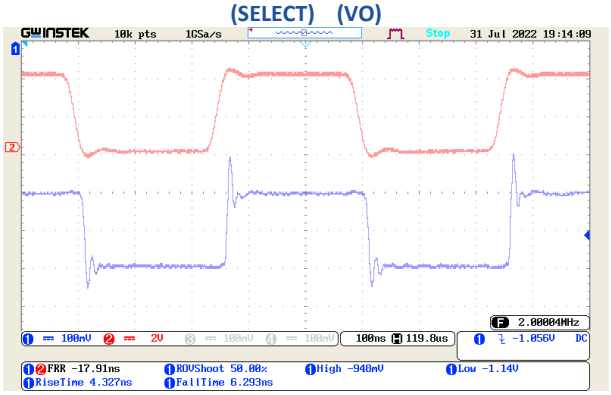
## Electrical Characteristics

$T_A$=25 °C, VDD_DIG=3.3 V, VSS=-4.5 V, $R_{REFH}$=3 KΩ, $R_{REFL}$=30 KΩ, $R_{REF1V}$=10 KΩ, $R_{HMON}$=2 KΩ, $R_{LMON}$=34.5 KΩ

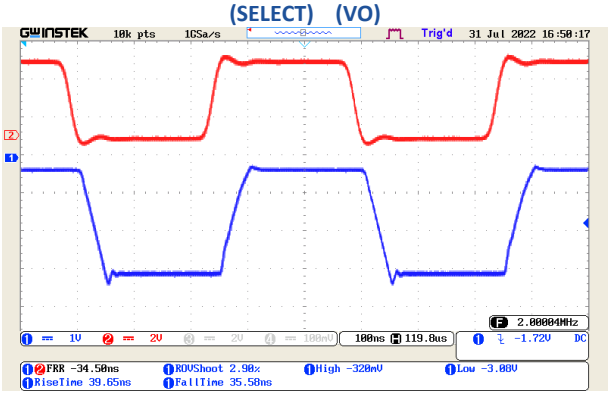
| Symbol | Parameter | Conditions | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $VREF_H$ | | | | -0.3 | | V |
| $VREF_L$ | | | | -2.995 | | V |
| $VREF_{HMON}$ | | | | -0.200 | | V |
| $VREF_{LMON}$ | | | | -3.492 | | V |
| $IREF_L$ | | | | 99.8 | | µA |
| $IREF_H$ | | | | 100.8 | | µA |
| $IREF_{LMON}$ | | | | 101.1 | | µA |
| $IREF_{HMON}$ | | | | 101.1 | | µA |
| $V_O$ | | Select = High<br>Select = Low | | -0.294<br>-3.000 | | V<br>V |
| $I_{IN-SELECT}$ | | Select = High<br>Select = Low | | 100<br>0 | | µA<br>µA |
| $V_{OL}$ | Output Voltage Lower-Level Swing | No Load<br>$I_{Load}$ = ±20mA | | -4.2<br>-4.2 | | V<br>V |
| $V_{OH}$ | | No Load<br>$I_{Load}$ = ±20mA | | -0.1<br>-0.1 | | V |
| $I_{SH}$ | Output Short Circuit | to GND<br>to VSS | | 30<br>23 | | mA |
| $I_{DD-Dig}$ | Digital Supply Current | No Load | | 2 | | mA |
| $I_{VSS}$ | Analog Supply Current | No Load | | 30 | | mA |
| $V_{SELECTH}$ | Select Digital High Level | | | 2.2 | | V |
| $V_{SELECTL}$ | Select Digital Low Level | | | 1.1 | | V |
| $t_{SEL-VOLH}$ | Select Up command to output $V_O$ 10% delay | FAST_EN = High, $C_L$ = 330pF<br>FAST_EN = Low, $C_L$ = 330pF<br>FAST_EN = High, $C_L$ = 20pF<br>FAST_EN = Low, $C_L$ = 20pF | | 13<br>25<br>8<br>14 | | ns<br>ns<br>ns<br>ns |
| $t_{SEL-VOHL}$ | Select Down command delay to output $V_O$ 10% delay | FAST_EN = High, $C_L$ = 330pF<br>FAST_EN = Low, $C_L$ = 330pF<br>FAST_EN = High, $C_L$ = 20pF<br>FAST_EN = Low, $C_L$ = 20pF | | 15<br>20<br>13<br>20 | | ns<br>ns<br>ns<br>ns |
| Slew rate | | FAST_EN = High<br>FAST_EN = Low | | 320<br>70 | | V/µs |
| $t_{DPG}$ | | Power good<br>Power Bad | | 95<br>0.3 | | ms<br>µs |
| $VOS_{MH}$ | $REFH_{MON}$ or $REFL_{MON}$ to $MON_{IN}$ offset voltage to remove PG flag | | | ±5 | | mV |
| $MON_{HYST}$ | | | | 25 | | mV |
| $PSRR_{VSS}$ | | VSS = 3V , 11V @ 10Hz | | 75 | | dB |
| $PSRR_{DIG}$ | | VDD_DIG = 2V , 5V @ 10Hz | | 93 | | dB |

## Gate Control Typical Performance Characteristics TA = 25◦ unless otherwise noted

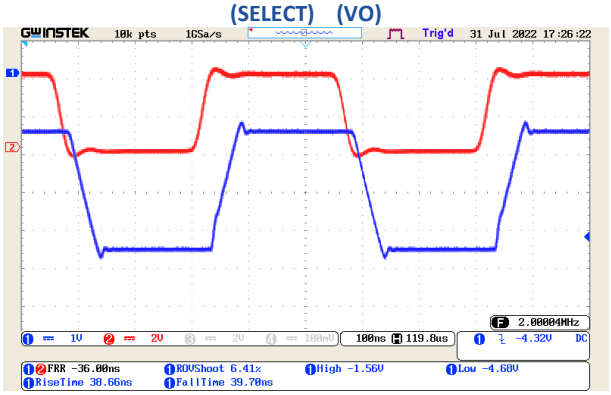
**small signal**
**-0.95V to -1.15V Step @ VSS=-6V, VDD_DIG = +3.3V FAST_EN = 0**
**RS = 0Ω, CL = 20pF, RL = 1KΩ**
**(SELECT) (VO)**



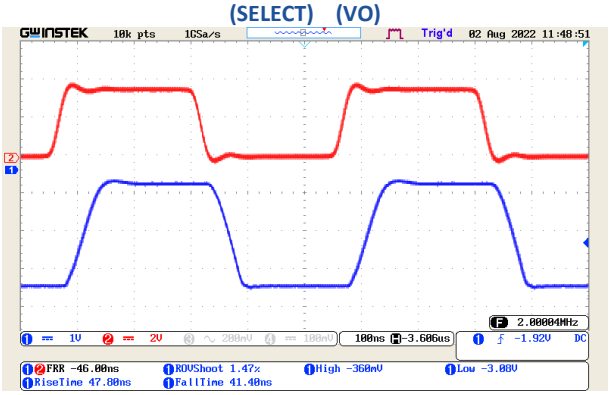

**Large signal**
**-0.3V to -3V Step @ VSS=-6V, VDD_DIG = +3.3V FAST_EN = 0**
**RS = 0Ω, CL = 20pF, RL = 1KΩ**
**(SELECT) (VO)**



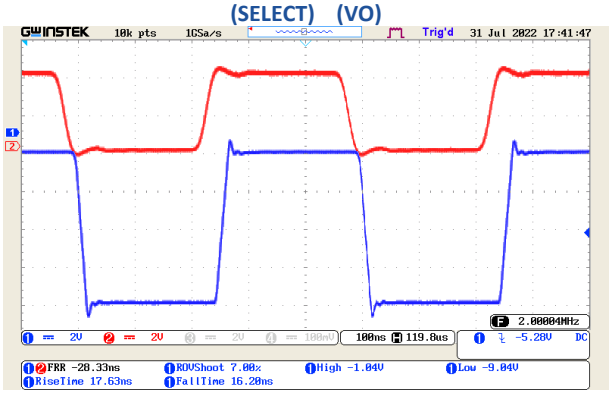

**Large signal**
**-1.5V to -4.5V Step @ VSS=-6V, VDD_DIG = +3.3V FAST_EN = 0**
**RS = 0Ω, CL = 20pF, RL = 1KΩ**
**(SELECT) (VO)**



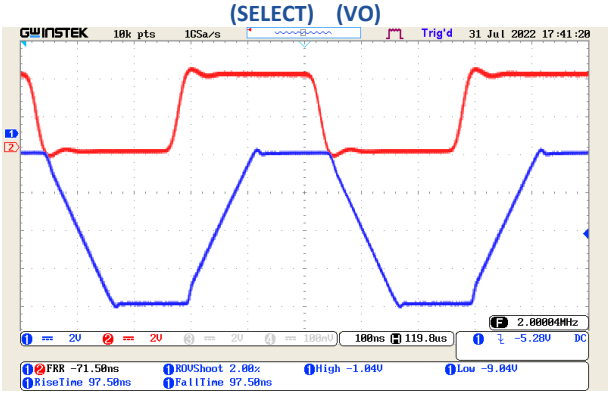

**Large signal**
**-0.3V to -3V Step @ VSS=-6V, VDD_DIG = +3.3V FAST_EN = 0**
**RS = 22Ω, CL = 330pF, RL = 1KΩ**
**(SELECT) (VO)**



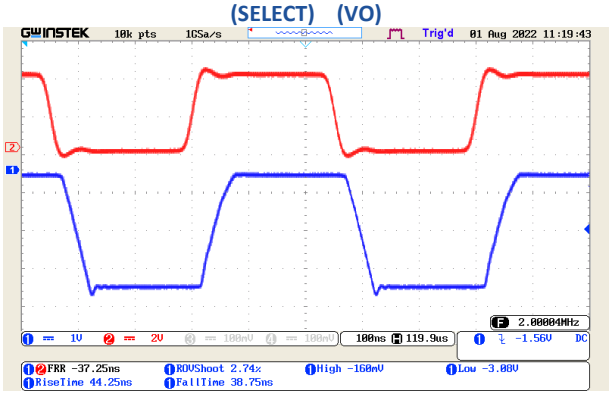

**large signal**
**-0.95V to -10.5V Step @ VSS=-12V, VDD_DIG = +3.3V FAST_EN = 1**
**RS = 22Ω, CL = 20pF, RL = 1KΩ**
**(SELECT) (VO)**



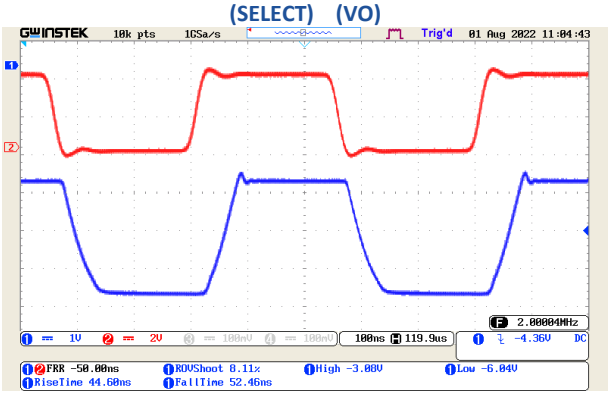

**large signal**
**-0.95V to -10.5V Step @ VSS=-12V, VDD_DIG = +3.3V FAST_EN = 0**
**RS = 0Ω, CL = 20pF, RL = 1KΩ**
**(SELECT) (VO)**



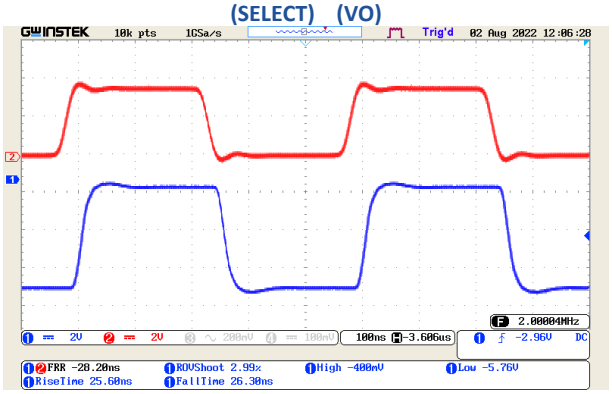
**Output Overdriven Recovery @ VSS=-6V, -0.16V to -3V, FAST_EN = 0**
**RS = 0Ω, CL = 20pF, RL = 1KΩ**
**(SELECT) (VO)**



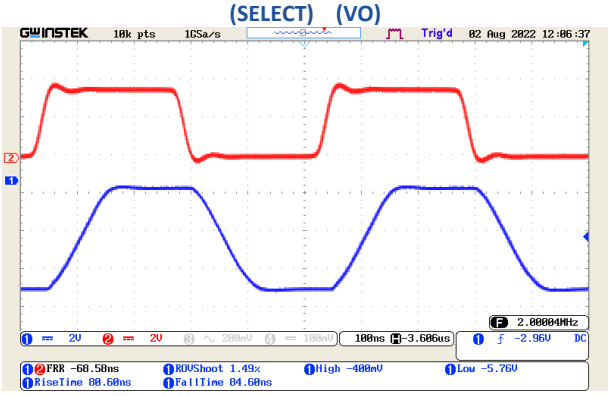

**Output Overdriven Recovery @ VSS=-6V, -3V to -6V, FAST_EN = 0**
**RS = 0Ω, CL = 20pF, RL = 1KΩ**
**(SELECT) (VO)**

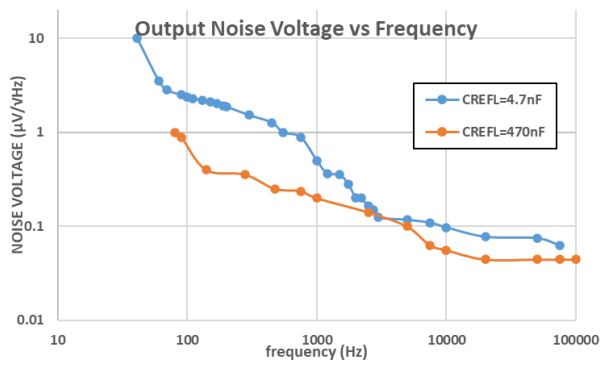


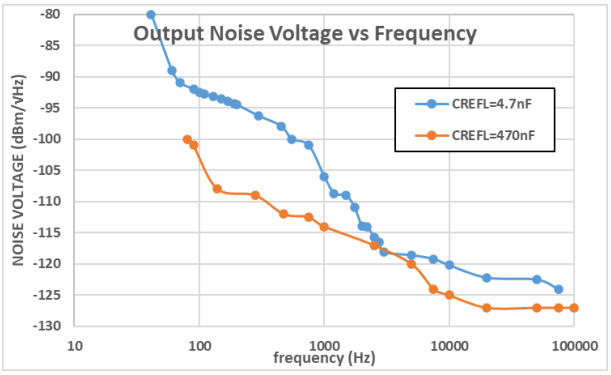

**Large signal**
**-0.3V to -5.5V Step @ VSS=-6V, VDD_DIG = +3.3V FAST_EN = 1**
**RS = 22Ω, CL = 330pF, RL = 1KΩ**
**(SELECT) (VO)**



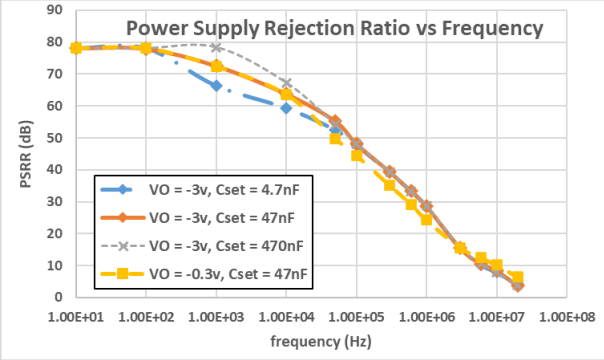

**Large signal**
**-0.3V to -5.5V Step @ VSS=-6V, VDD_DIG = +3.3V FAST_EN = 0**
**RS = 22Ω, CL = 330pF, RL = 1KΩ**
**(SELECT) (VO)**



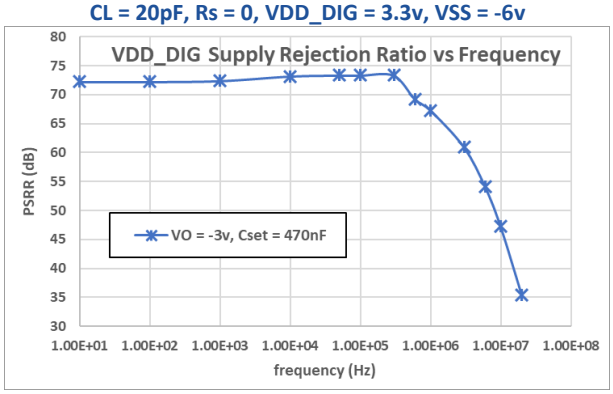



CL = 20pF, Rs = 0, VDD_DIG = 3.3v, VSS = -6v




CL = 20pF, Rs = 0, VDD_DIG = 3.3v, VSS = -6v



## Pin Functions

**VDD0:** Ground. Tie these pads to local ground plate on PCB. To ensure proper electrical and Thermal performance connect all pins with wide polygon to ground.

**VSSL:** The VSSL pin supplies current to the ASNGC4X20's internal Output Buffer and to the internal reference block. This pin must be locally bypassed with an external, low ESR capacitor of at least 4.7µF. The VSSL pin voltage level is negative and should be set between -3V to -12V for best chip performance.

**VDD_DIG:** The VDD_DIG pin supplies current to the ASNGC4X20's internal Select input section and to the internal monitoring block. This pin must be locally bypassed with an external, low ESR capacitor of at least 1µF. The VDD_DIG pin voltage level is positive and should be set between 2.5V to 5V for best chip performance.

**$REFL_{MON}$, $REFH_{MON}$:** ASNGC4X20 Monitoring Reference pads. For $R_{REF1V}$ equal to 10Kohm, a fixed current of 100µA flows into these pins through a single external resistor ($R_{HMON}$, $R_{LMON}$) connected between ground and each pad, which sets a negative voltage on each pad to program the monitoring reference levels. For correct function of monitoring block, the value of $R_{LMON}$ must be selected greater than $R_{HMON}$ ($REFL_{MON}$ pin voltage must be lower than $REFH_{MON}$). In order to reject high frequency noise a parallel capacitor ($C_{HMON}$ and $C_{LMON}$) can be used with $R_{HMON}$ and $R_{LMON}$. Do not use more than 10nF for $C_{HMON}$ and $C_{LMON}$.

**REFL, REFH:** ASNGC4X20 Output voltage levels Reference pads. For $R_{REF1V}$ equal to 10Kohm, a fixed current of 100µA flows into these pins through a single external resistor ($R_{REFH}$, $R_{REFL}$) connected between ground and each pad, which sets a negative voltage on each pad to program the output voltage reference levels. The value of $R_{REFH}$ must be selected greater than $R_{REFL}$ (REFL pin voltage must be lower than REFH). In order to reject high frequency noise a parallel capacitor ($C_{REFH}$ and $C_{REFL}$) can be used with $R_{HMON}$ and $R_{LMON}$. Do not use more than 1µF for $C_{REFH}$ and $C_{REFL}$.

**REF1V:** Current Reference pad. A 1.01V is internally applied between this pad and VSSL. Connect a 1% 10K resistor between this pad and VSSL to set a 101uA reference current that flows into REFL, REFH, $REFH_{MON}$ and $REFL_{MON}$ pads.

**$FAULT_{RSTX}$:** Monitoring digital output flag. The pad output High level voltage is VDD_DIG and Low logical level voltage is 0V. The pin output level is High if $MON_{INX}$ voltage is between $REFL_{MON}$ and $REFH_{MON}$ and is Low otherwise. High to Low transition of this pad happens immediately (300ns delay) and at $MON_{INX}$ lower than $REFL_{MON}$ or greater than $REFH_{MON}$ and Low to High transition happens with a typical 95ms delay after

$REFLMON+25mV < MON_{INX} < REFH_{MON}-25mV$

**$MON_{INX}$:** Monitoring input. This pad should be connected in remote sense condition (without current) to a negative voltage relative to ground. The function of monitoring is explained above. Two protection diode is internally connected between this pad and VSSL/VDD0 pads so the applied voltage on $MON_{INX}$ pad must be between ground and VSSL.

**$VO_X$:** ASNGC4X20 output pad. This pad is internally driven by a unity gain amplifier with 60MHz bandwidth, a 70V/us (Up to 320V/us by FST_EN) slew rate and a 70deg phase margin at 20pF capacitive load. The maximum output capacitive load is 50pF for stability. For more capacitive loads connect a 22Ω series resistor (RS) in the output. The output current limit is 23mA DC and 500mA peak (less than 200ns). This pad voltage level is set by REFH and REFL pads. The $VO_x = V_{REFL}$ if SELECT=Low and $VO_X=V_{REFH}$ if SELECT=High.

**SELECT:** ASNGC4X20 digital input. The pad input High level voltage is VDD_DIG and Low level is 0V. This pad sets $VO_X$ voltage level on REFH and REFL voltage. The $VO_x = V_{REFL}$ if SELECT=Low and

$VO_X$=$V_{REFH}$ if SELECT=High. SELECT is internally protected for input voltages above VDD_DIG and below 0V. Minimum input pulse width is 60ns. This pad is internally pulled down.

**FST_EN:** Fast operation mode enable pad. In fast operation mode the supply current of the ASNGC4X20 increases to about 5 time more than typical condition within 20ns after the SELECT input is toggled so the outputs slew rate increases to 320V/us. The current usage is not changed in Fast mode when the SELECT is fixed. Fast mode operation is recommended in large output steps as high as 3V or more. Fast mode operation increases the pulse current drawn from VSSL when SELECT input is toggled and should be considered in sensitive application. This pad is internally pulled down.

**THERMAL_FLAG:** Over temperature output digital flag pad. The pad output Low and High voltage levels are 0V and VDD_DIG, respectively. The output is Low when the temperature is below 180$^o$C and is high otherwise.

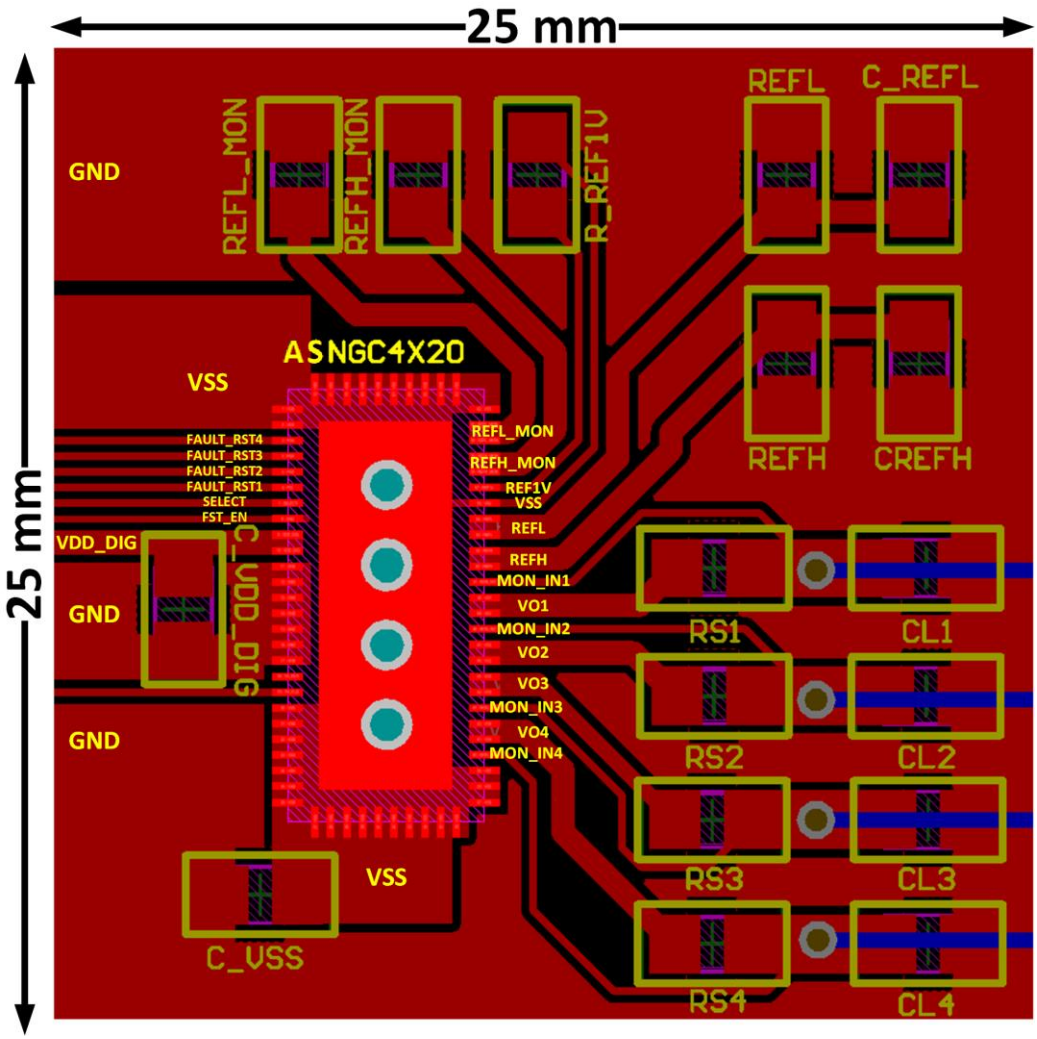
**THERMAL_REACT_EN:** Over temperature reaction enable pad. This pad is a pulled up digital input. Tie it to VDD0 to disable the Over temperature reaction mode and leave it to enable that. In Over temperature reaction enable mode, the supply current usage and outputs current limit level decreases by 80% while the chip internal temperature is increased above 180$^o$C. This pad is internally pulled up.

## Application Information

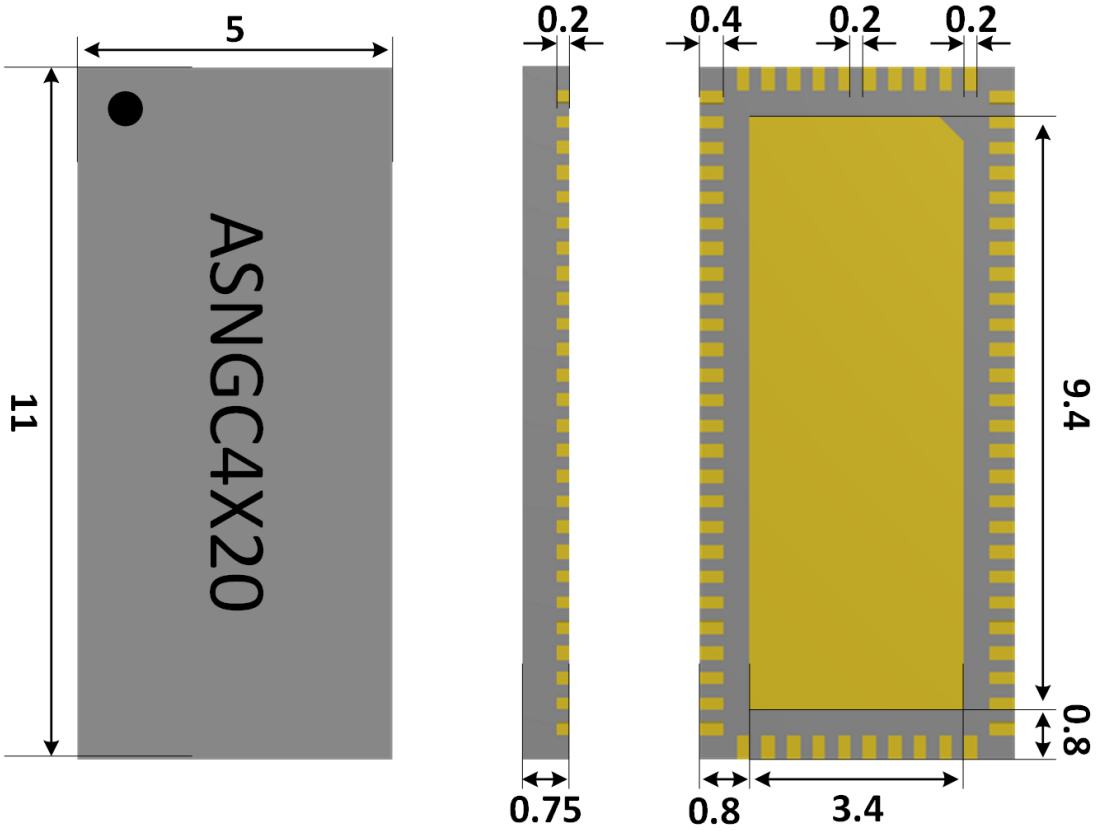
### PCB Layout

The ASNGC4X20 includes quad negative gate control and monitor. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 3 for a suggested layout. Ensure that the grounding and heat sinking are acceptable. A few rules to keep in mind are:

1. Place the $R_{REFL}$, $R_{REFH}$, $R_{REFHMON}$, $R_{REFLMON}$ and $R_{REF1V}$ resistors as close as possible to their respective pins.
2. Place the $C_{REFH}$ and $C_{REFL}$ capacitors as close as possible to their respective resistors.
3. Place the RS resistors as close as possible to their respective pins.
4. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the ASNGC4X20.
5. CL capacitors can be placed far from the ASNGC4X20 if RS resistors have been used.
6. It is recommended to connect MON_IN track without DC current path to monitor the consumer voltage level.
7. Use vias to connect the GND copper area to the board's internal ground plane. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board.



## All dimensions are in mm ± 0.05 mm




72 pin QFN Package