ASN1010

36 V, 1 A EM Compliant Switching Regulator with a Configurable LDO

Features

- **Inverting Switch Mode Power Supply**
- **Wide Input Voltage Range: 8 V to 36 V**
- **1 A Buck-boost Output Current**
- **-2 V to -12.5 V Output Voltage**
- **Selectable Switching Frequency: 0.2 MHz to 2.5MHz**
- **Adjustable 10% Accurate Current Limit**

– Single 1 A LDO Regulator

– Output Adjustable From 0 V to -12 V

– Low Output Noise: 10µvrms (10 Hz to 100 kHz)

- **Programmable Soft-Start**

Applications

- Automotive Battery Regulation
- RF Transceivers

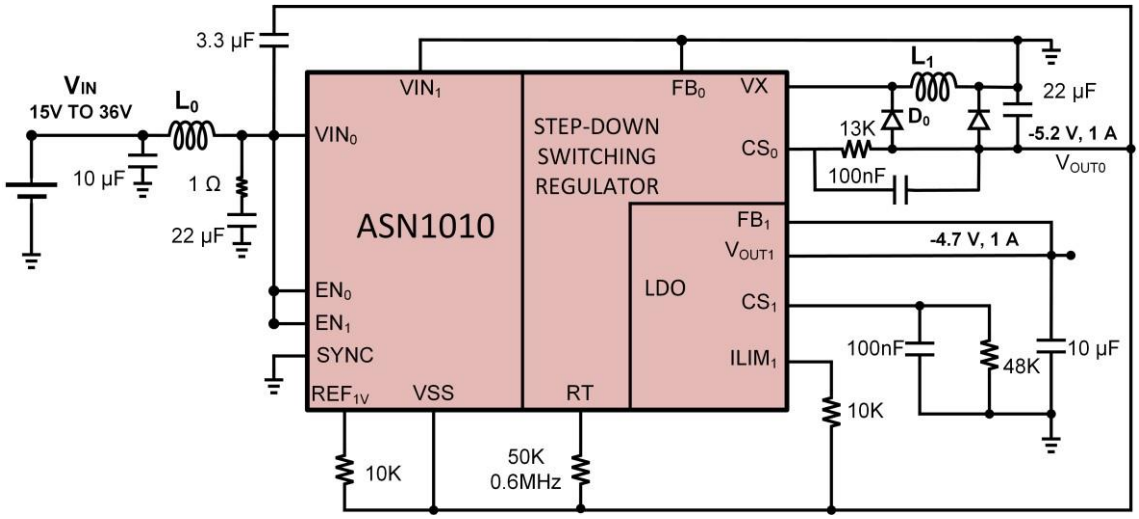
Description

The ASN1010 is a 36 V, 1 A step-down High-Side switch and regulator controller chip with a configurable LDO. Operating over an input voltage range of 8V to 36V, the ASN1010 Buck-boost regulator supports an output voltage range of -2 V to -12.5 V and wide selectable switching frequency range of 200 kHz to 2.5 MHz each set by a single resistor. The Buckboost regulator has synchronization possibility and generates low switching noise. Following the Buckboost regulator is a 1A linear regulator.

The ASN1010 is packaged in thermally enhanced QFN package and has high efficiency which makes it a good solution for high density power management units.

Typical Application

1A Output DC/DC Converter



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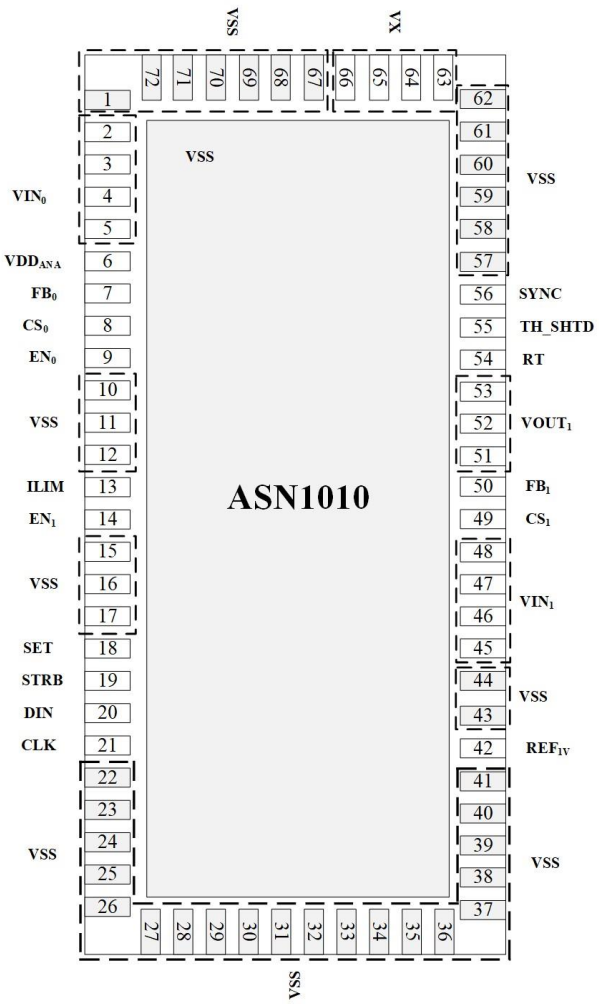
Absolute Maximum Rating

VIN_0, VDD_{ANA}, VX..... 45 V
EN_0, EN_1, TH_SHTD ..... 36 V
FB_0, SYNC, RT, CS_0,CS_1, REF_{1V} ..... 5.5 V
$ILIM_1$ ..... 5.5 V
SET, STRB, DIN, CLK 5.5V
VIN_1 ..... 13 V
FB_1 ..... 13 V
$VOUT_1$ ..... 13 V
Maximum Junction Temperature..... 200 °C

Pin Configuration



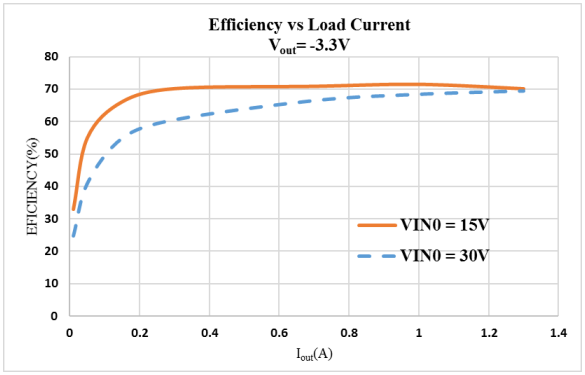
Electrical Characteristics

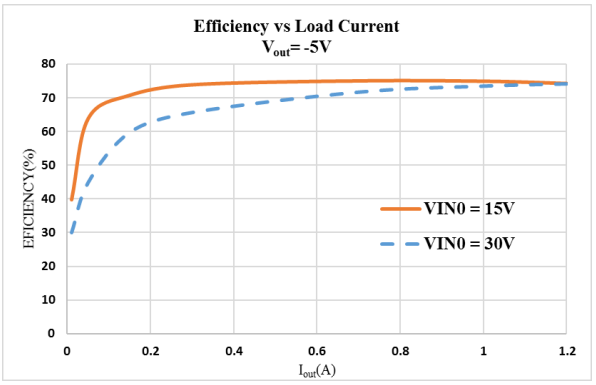
Parameter	Conditions	MIN	TYP	MAX	UNITS
Buck-boost Regulator					
Minimum VIN_0 Input Voltage		7.5		8.5	V
Buck-boost $VOUT_0$ DC Voltage	0 A < I_{out} < 1 A R_{CS0} = 5kΩ 0 A < I_{out} < 1 A R_{CS0} = 30kΩ		-2 -12		V V
Quiescent Current into VIN_0	EN_0, EN_1, EN_2 = 0		7		mA
$VOUT_0$ Line Regulation	8V < VIN_0 < 36V, I_{out} = 1 A		±0.5		%
$VOUT_0$ Load Regulation	VIN_0 = 28V, 0A < I_{out} < 1 A		±1		%
$VOUT_0$ RMS Voltage Ripple	VIN_0 = 28V, $VOUT_0$ = 3.3V, 0A < I_{out} <1A		4.5		mV

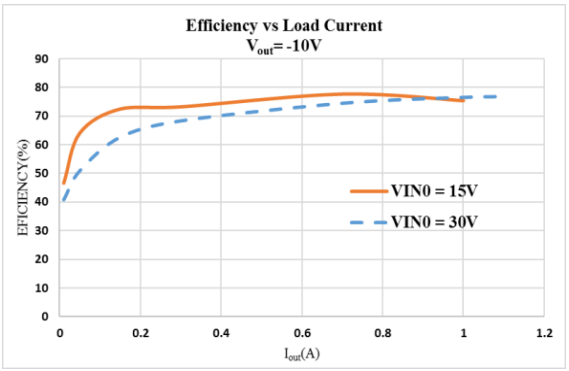
$VOUT_0$ RMS Output Noise	$VOUT_0$ = 5V, I_{Load} = 1A, C_{CS0} = 10nF 10Hz to 100kHz		180		µV
$VOUT_0$ RMS Output Noise	$VOUT_0$ = 5V, I_{Load} = 1.4A, C_{CS0} = 100nF 10Hz to 100kHz		160		µV
Switching Frequency	RT = 28k RT = 156k		1000 200		kHz kHz
EN_0 Threshold Voltage	OFF			0.5	V
EN_0 Threshold Voltage	ON	1			V
CS_0 Pin Current	R_{ref} = 10k	98	100	102	µA
RT Pin Voltage		0		5	V
SYNC Input Low Threshold				0.5	V
SYNC Input High Threshold		1			V
LDO					
CS_1 Pin Current	R_{ref} = 10k	98	100	102	µA
REF_{1V} Pin Voltage		0.99	1.01	1.03	V
LDO Dropout Voltage	I_{Load} = 100mA I_{Load} = 700mA		0.1	 0.200	V V
LDO Maximum Dropout Voltage	R_{LIM} = 19k, I_{Load} = 390mA R_{LIM} = 19k, I_{Load} = 700mA R_{LIM} = 19k, I_{Load} = 950mA			-12 -7.5 -4.5	V V V
$VOUT_1$ RMS Output Noise	$VOUT_1$ = 3.3V, I_{Load} = 400mA, 100Hz to 100kHz, C_{CS1} = 47nF		28		µV
$VOUT_1$ RMS Output Noise	$VOUT_{1,2}$ = 3.3V, I_{Load} = 400mA, 100Hz to 100kHz, $C_{CS1,2}$ = 470nF		8		µV
EN_1 Threshold Voltage	OFF			0.5	V
EN_1 Threshold Voltage	ON	1			V

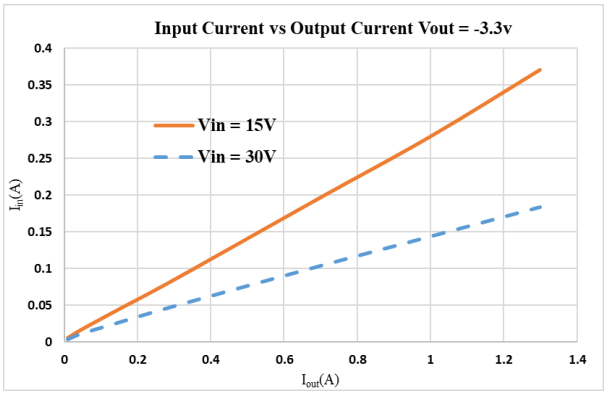
DC/DC conv. Typical Performance Characteristics

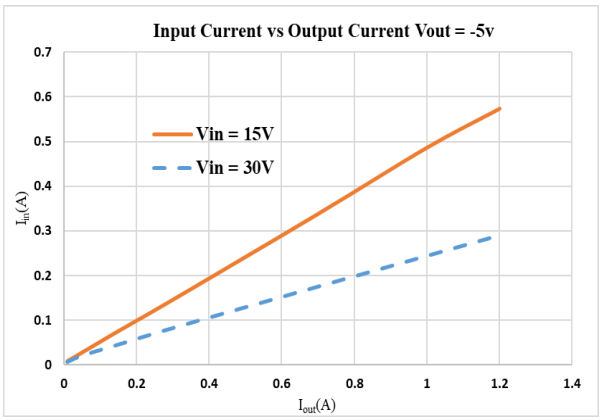
TA = 25◦ unless otherwise noted

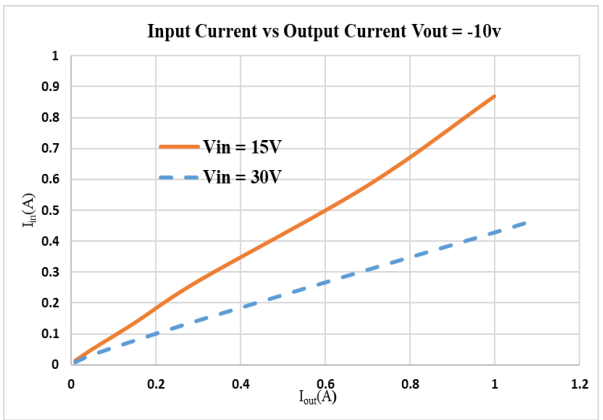






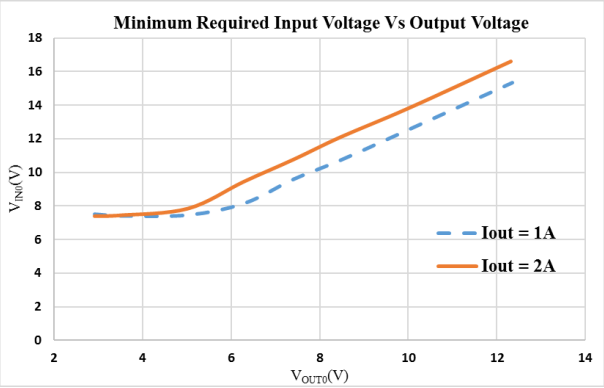


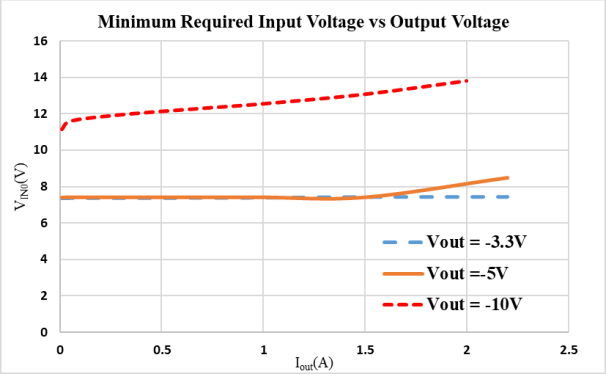


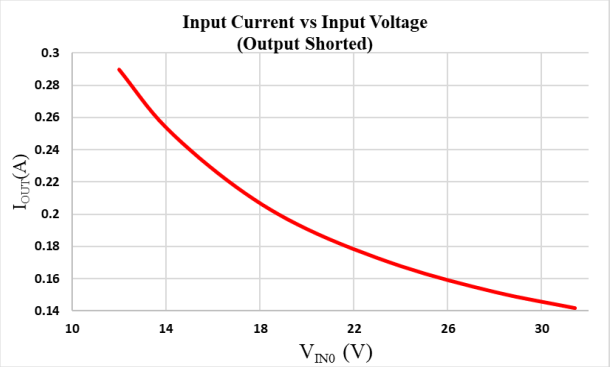


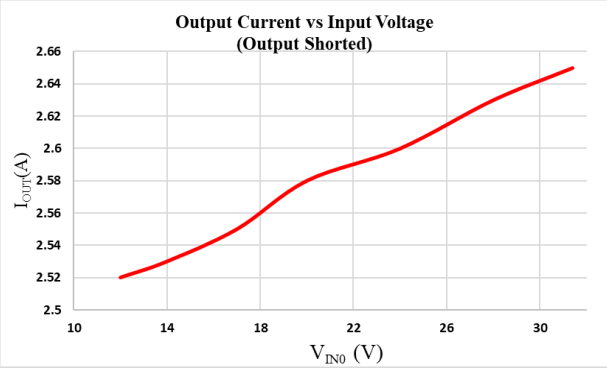
DC/DC conv. Typical Performance Characteristics

TA = 25◦ unless otherwise noted

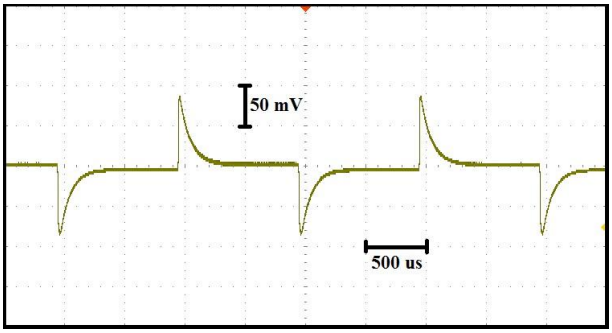








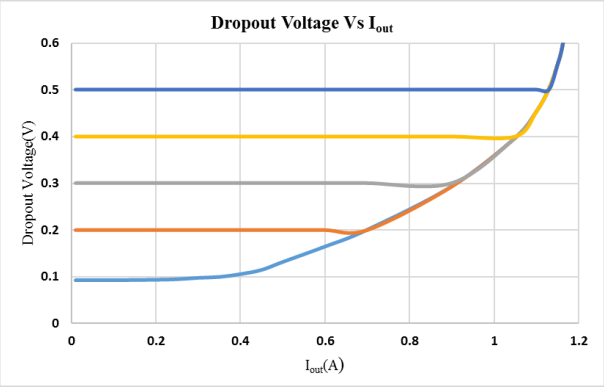
Load Transient Response $IOUT_1$ = 200 mA ~ 700 mA

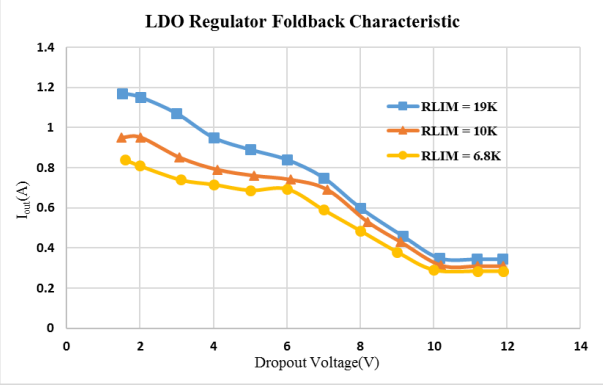


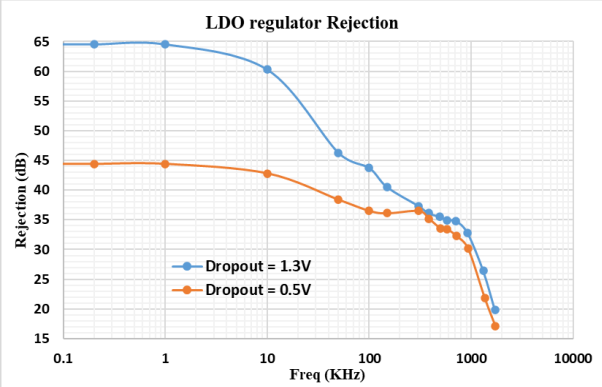
$VOUT_0$ = -5 V, C_{OUT-BK} = 22 µF

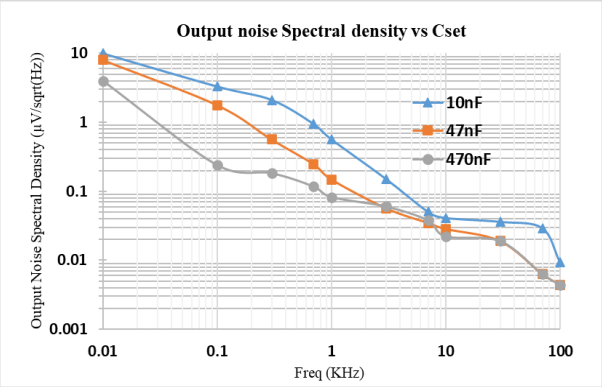
LDO Typical Performance Characteristics

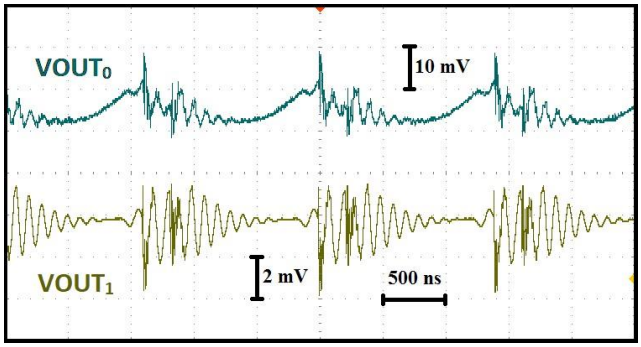
TA = 25◦ unless otherwise noted



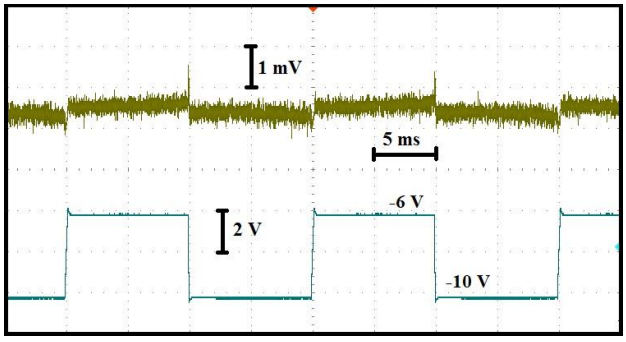






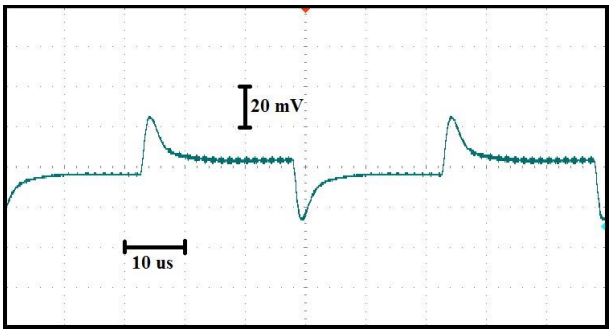


$VOUT_0$ = -5 V, C_{OUT-BK} = 22 µF
$VOUT_1$ = -4 V, $C_{OUT-LDO}$ =10 µF
I_{OUT1} = 400 mA (Buck-boost loaded with LDO)



$VOUT_1$ = -3.3 V, $C_{OUT-LDO}$ = 10 µF
I_{OUT1} = 400 mA (Buck-boost loaded with LDO)

Load Transient Response $IOUT_1$ = 200 mA ~ 600 mA



$VOUT_0$ = 5 V, C_{OUT-BK} = 22 µF $VOUT_1$ = 4 V, $C_{OUT-LDO}$ = 10 µF

Pin Functions

VIN0: The VIN0 pin supplies current to the ASN1010's internal power switch. This pin must be locally bypassed with an external, low ESR capacitor of at least 4.7µF. It's recommended to use low EMI filter before VIN pin as mentioned in application information.

VDD_{ANA}: The VDDANA pin supplies current to the ASN1010's internal regulator. This pin can be connected to the VIN0 pin or a higher than 8V supply voltage with 10mA current capability.

VX: DC/DC converter High-side switch drain. This pad should connect to converter Output filter inductor and Diode in a structure with low electromagnetic emission (refer to PCB Layout recommendation section).

VSS: Chip lowest voltage node. Tie these pads to local ground plate on PCB. To ensure proper electrical and Thermal performance connect all pins with wide polygon. When buck-boost regulator this node is the buck-boost output voltage.

VIN1: linear regulator input. Tie these pads to local ground plate on PCB.

FB_0, FB_1: Regulator VOUT feedback. Connect these pads to regulator output node, which want to be regulated. To have a well-regulated voltage use a remote sense connection of this pad to output node. Avoid to near switching tracks to feedback track.

REF_{1V}: Reference 1 V pad. This pin has a 1 V fixed reference voltage, which makes 100 µA fixed current on the 10 kΩ external connected resistor. This current is mirrored in the chip to generate C_{SET0} and C_{SET1} pins current. If another value is used for REF_{1V} resistor C_{SET0} and C_{SET1} pins current will be

$$I_{SET} = \frac{1\,V}{R_{REF1v}}$$

and regulators' output voltage should be calculated based on this current. Do not connect less than 5 kΩ resistor to this pin.

C_{SET0}, C_{SET1}: These pins set the regulation point for each regulator. For R_{REF1V} equal to 10Kohm, A fixed current of 100µA flows out of these pins through a single external resistor (R_{CS0}, R_{CS1}), which programs the output voltage of each regulator. Output voltage range is from -2V to 12.5V for Buck-boost regulator and 0V to -12V for LDO. The required resistor from the formula:

$$R_{CS0} = \frac{10}{4} \times |V_{OUT}|\ k\Omega$$

$$R_{CS1} = 10 \times |V_{OUT}|\ k\Omega$$

Furthermore, these pads control the regulators output voltage soft start speed and output noise spectrum, using a capacitor. Soft start duration is a function of C_{CS} capacitor:

$$T_{SOFT-START} = 4 \times R_{CS} \times C_{CS}$$

$ILIM_1$: External Current Limit Programming. This pin externally programs current limit with following function relative to R_{LIM} (kΩ) resistor connected from this pin to VSS:

$$I_{LIM} = 0.8\frac{R_{LIM}}{5.3 + R_{LIM}} + 0.4(A)$$

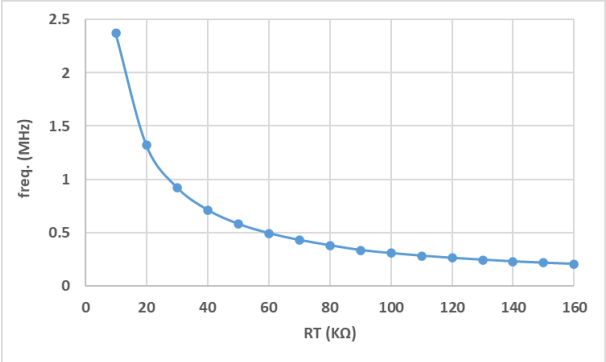
EN_0, EN_1: Regulator Enable pin. Switching regulator is enable if relative EN_0 pin voltage level to GND is more than 1V and has 0.1V hysteresis window for disable. LDO regulator is enable if relative EN_1 pin voltage level to GND is more than 1 V or less than -1 V. EN_1 has 0.1 V hysteresis window on both sides. These pins are internally pull down to GND with 100Kohm resistor.

SYNC: This is the external clock synchronization input. Tie to a clock source for synchronization. Clock edges rise time and fall time should be faster than 1µs and its voltage amplitude must be larger than 1.2V peak-to-peak. The internal oscillator of the ASN1010 can be synchronized by applying an

external 250 kHz to 2MHz clock to the SYNC pin. The resistor tied from the RT pin to ground should be chosen such that the ASN1010 oscillates 20% lower than the intended synchronization frequency. Do not leave this pin float.

RT: The RT pin is used to program the switching frequency of the ASN1010 by connecting a resistor from this pin to VSS.

RT (kΩ)	Freq. (kHz)
12	2000
22.5	1500
28	1000
39	750
82	375
125	250



$VOUT_1$: LDO Output. This pin supply power to the load. Stability requirements demand 10µF ceramic output capacitor with an ESR less than 100mΩ to prevent oscillations.

TH_SHDN: Thermal shutdown flag. This pin generates the thermal shutdown 5 V signal when the chip temperature reaches 185°C. in addition, TH_SHDN flag disables all regulators and enables them again when the chip temperature decreases to 165°C. This pin can be tied to VSS if user does not need thermal shutdown reaction.

SET, STRB, DIN, CLK: These pins are used for productions tests. Tie these pins to VSS.

VIN_0	$VOUT_0$	C_{OUT}	R_{CS0} (kΩ)	f_{opt} (kHz)	RT_{opt} (kΩ)	f_{MAX} (kHz)	RT_{MIN} (KΩ)
8V ~ 35V	-1.50V	22μF 1206	3.75	400	50	700	43
8V ~ 35V	-2.5V	22μF 1206	6.25	600	75	900	33
8V ~ 15V	-3.5V	22μF 1206	8.75	850	35	1000	33
15V ~ 35V	-3.5V	22μF 1206	8.75	750	40	900	30
8V ~ 35V	-4.5V	22μF 1206	11.25	850	35	1000	30
8V ~ 20V	-5.5	22μF 1206	13.75	1000	30	1200	25
20V ~ 35V	-5.5	22μF 1206	13.75	900	33	1100	27
8V ~ 15V	-6.5	22μF 1206	16.25	950	32	1200	25
15V ~ 35V	-6.5	22μF 1206	16.25	850	35	1000	30
10V ~ 15V	-7.5	22μF 1206	18.75	1000	30	1200	25
15V ~ 35V	-7.5	22μF 1206	18.75	850	35	1100	27
12V ~ 20V	-8.5	22μF 1206	21.25	1100	27	1200	25
20V ~ 35V	-8.5	22μF 1206	21.25	900	33	1100	27
12V ~ 20V	-10	22μF 1206	25	1200	25	1200	25
20V ~ 35V	-10	22μF 1206	25	950	32	1100	27

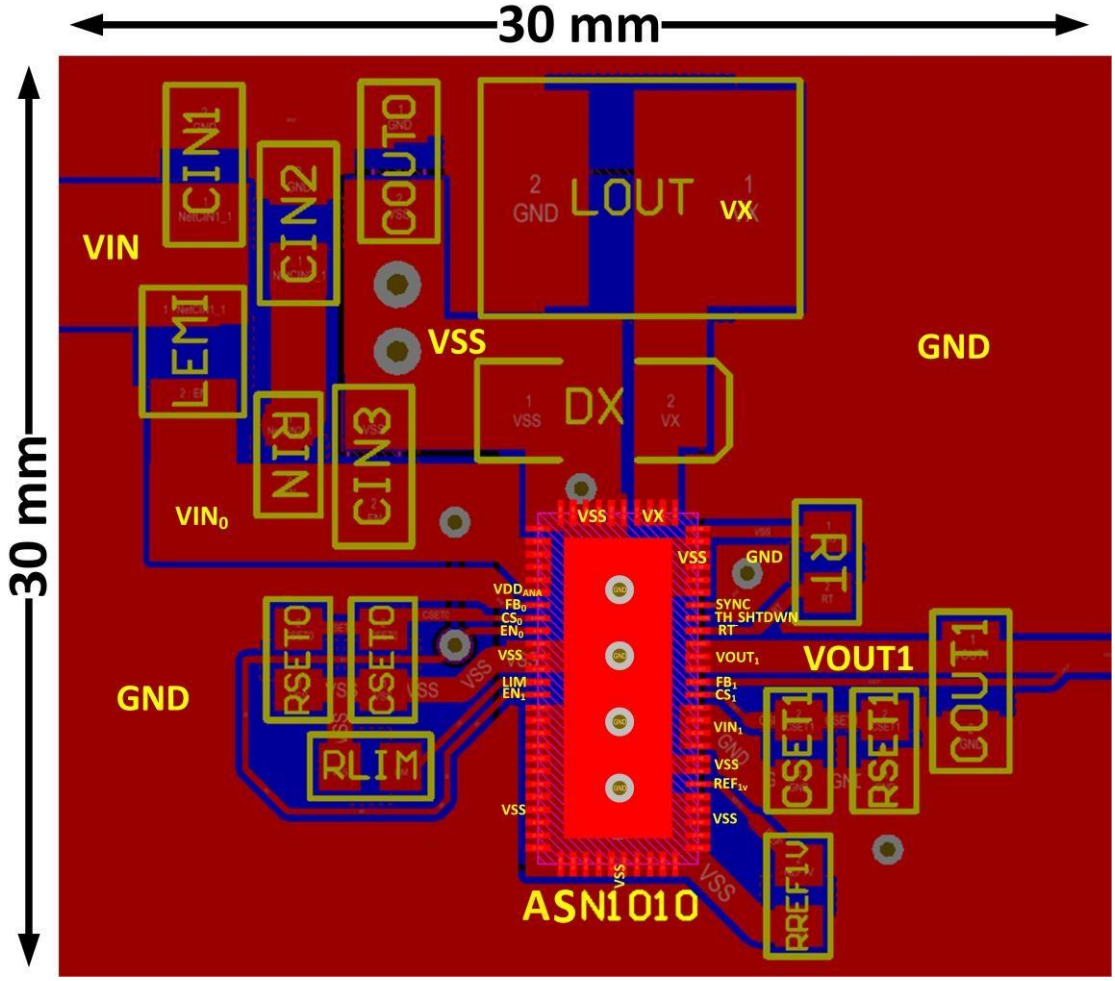
Application Information

PCB Layout

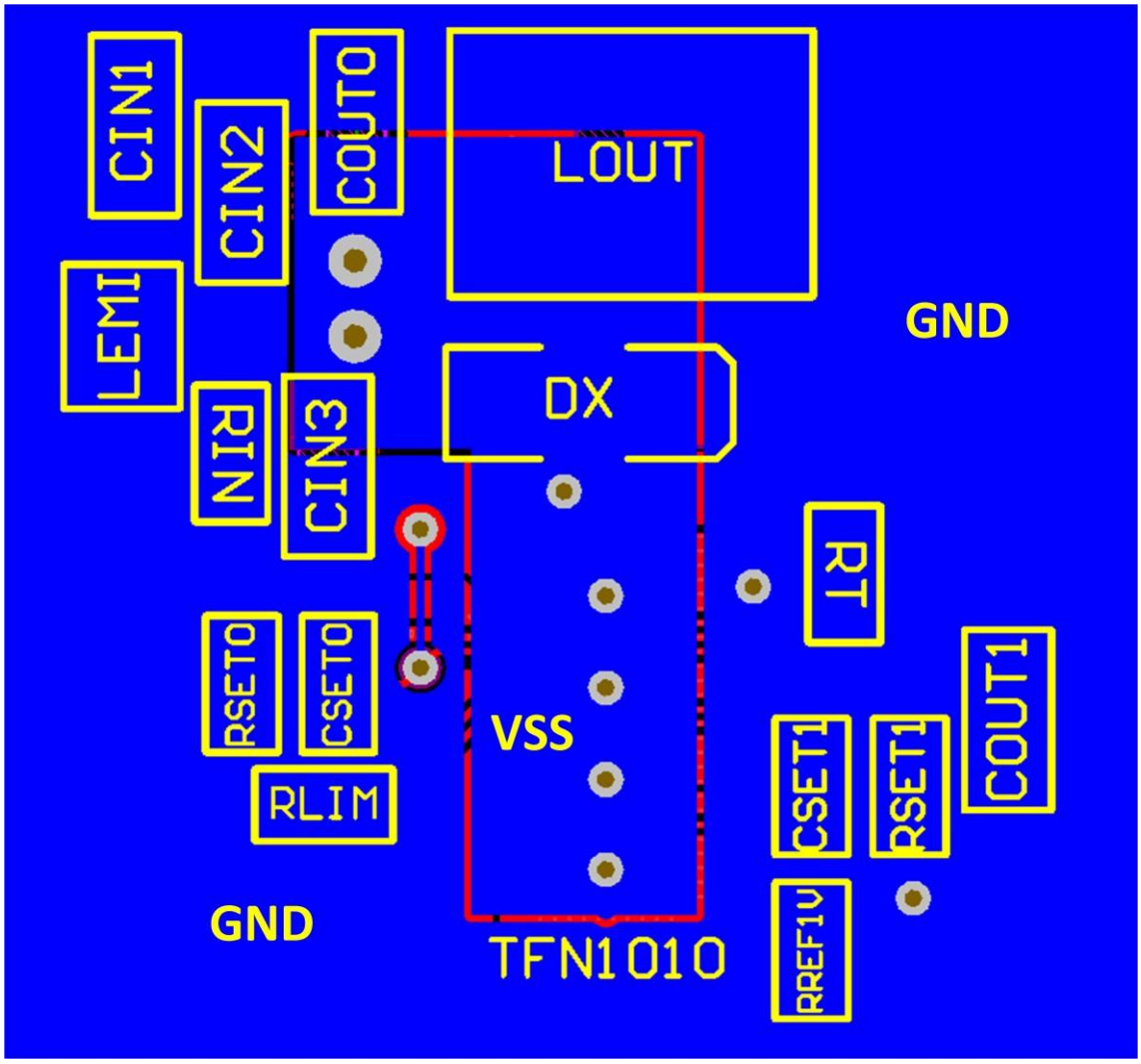
The ASN1010 includes a switching power supply and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 3 for a suggested layout. Ensure that the grounding and heat sinking are acceptable. A few rules to keep in mind are:

1. Place the R_{CS0}, R_{CS1} and RT resistors as close as possible to their respective pins.
2. Place the C_{IN} capacitor as close as possible to the VIN and GND connection of the ASN1010.

3. Place C_{OUT} capacitors as close as possible to relative VOUT and GND connection of the ASN1010.
4. Place the C_{IN} and C_{OUT} capacitors such that their ground currents flow directly adjacent or underneath the ASN1010.
5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the ASN1010.
6. Use via to connect the VSS copper area to the board's internal VSS plane. Liberally distribute these VSS vias to provide both a good VSS connection and thermal path to the internal planes of the printed circuit board.

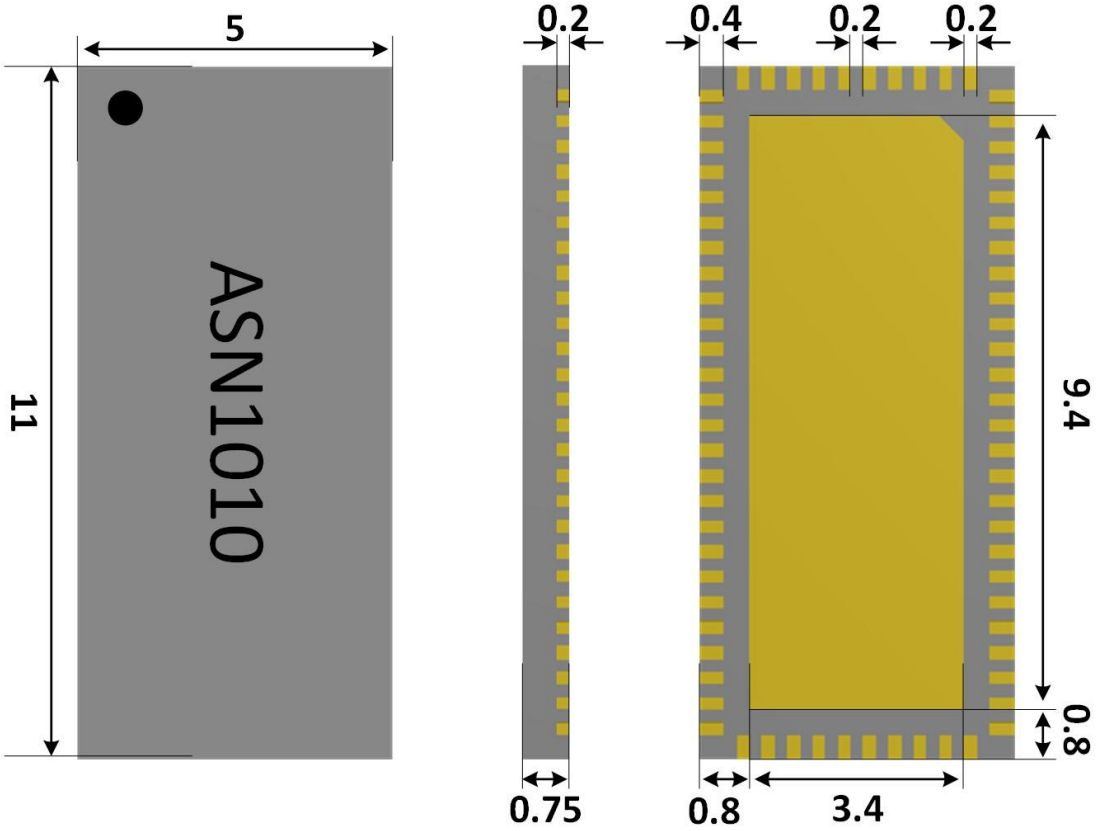


Top View


CIN1
CIN2
COUTO
LOUT
LEMI
GND
RIN
CIN3
DX
RT
RSETO
CSETO
VSS
COUT1
CSET1
RSET1
RLIM
GND
TFN1010
RREF1V

Bottom View

All dimensions are in mm ± 0.05 mm



72 pin QFN Package

Recommended Off-chip Components

Component	Value	Manufacturer	Recommended Part Number
D_1	--	ONSEMI ST	MBRS360BT3G STPS3H60-Y
L_1	4.7 µH	Coil Craft Coil Craft	XAL5030-472ME XGL6030-472ME
L_0	4.7 µH	TDK	252012ALMA4R7MTAA