1. Introduction

The AS4275 is a monolithic integrated low-dropout voltage regulator offered in a 5-pin TO-252 package. The device regulates an input voltage up to 45V to V_{OUT} = 5V (typical). The IC can drive loads up to 450 mA and is short-circuit proof. At over-temperature, the AS4275 is turned off by the incorporated temperature protection. The device would generate a reset signal for an output voltage, V_{Out} of a typical 4.65V. By the use of an external delay capacitor, one can program the reset delay time.

2. Features

- Suitable for use in automotive electronics
- AEC qualified
- Output voltage 5 V (± 2%)
- Very low dropout voltage
- Very low current consumption
- Power-on and undervoltage reset
- Reset low-level output voltage < 1 V
- Short-circuit proof
- Reverse-polarity proof
- ESD protection > 4 kV

3. Applications

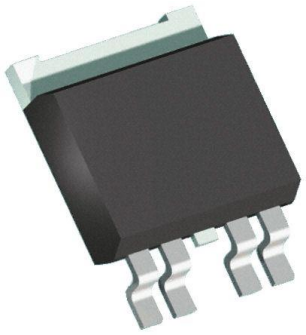
- Qualified for automotive applications
- Cluster
- Body control modules
- Heating Ventilation and Air Conditioning (HVAC)

3.1 Description

The input capacitor, C_{IN}, is necessary for compensation of line fluctuation. Using a resistor of approximately 1 Ω in series with C_{IN} dampens the oscillation of input inductance and input capacitance. The output capacitor, C_{OUT}, is necessary for the stability of the regulation circuit. Stability is guaranteed at values C_{OUT} ≥ 22 µF and an ESR ≤ 5 Ω within the operating temperature range. Stability for electrolytic capacitors specifically is at C_{OUT} ≥ 68 µF within the operating temperature range.

The control amplifier compares a reference voltage to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any oversaturation of the power element. The IC also incorporates a number of internal circuits for protection against:

- Overload
- Overtemperature
- Reverse polarity



AS4275
5-PIN TO-252

4. Pin configuration

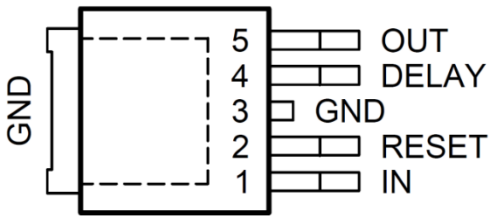


Figure 1: Pin configuration

Symbol	Type	Description
IN	I	Input, connect to ground through a ceramic capacitor as close to device as possible
RESET	I	Reset output, open collector output
GND	O	Ground, short pin internally connected to heatsink
DELAY	O	Reset delay, connect to ground with a capacitor to set delay time
OUT	O	Output, connect to ground with Capacitor ≥ 22 µF and ESR < 5 Ω at 10 kHz

5. Ordering information

Part number	Package		
	Name	Description	Version
AS4275	TO-252	Plastic flange-mount package; 5 pins	-

6. Block diagram

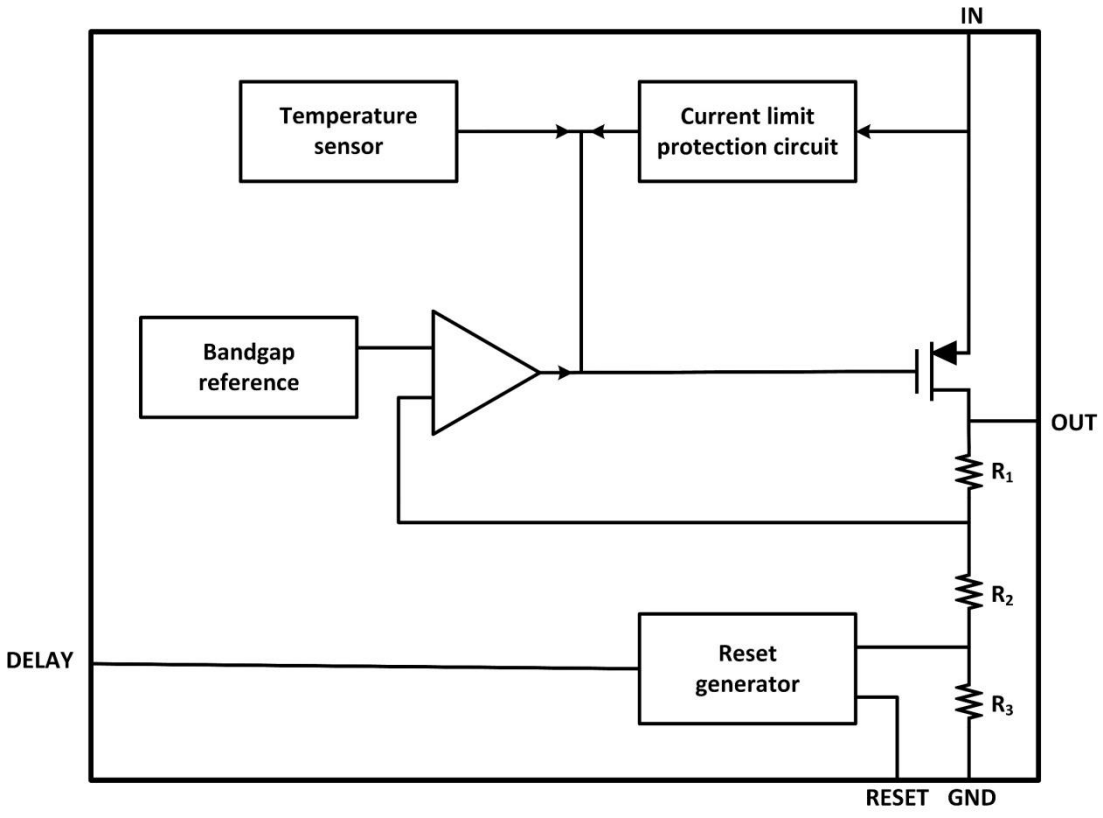


Figure 2: Block diagram

7. Absolute maximum ratings[1]

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_I	Input voltage range[2]	On pin IN	0	-	45	V
		On pin DELAY	-0.3	-	5.5	V
V_O	Output voltage range	On pin OUT	-1	-	5.5	V
		On pin RESET	-0.3	-	5.5	V
I_I	Input current	On pin DELAY	-2	-	+2	mA
I_O	Output current	On pin RESET	-5	-	+5	mA
T_J	Operating junction temperature		-40	-	150	°C
T_{stg}	Storage temperature		-65	-	150	°C
$V_{(ESD)}$	Electrostatic discharge	IEC61000-4-2[3]				
		OUT and IN	-6	-	+6	kV
		All other pins	-2	-	+2	kV

8. Recommended operating conditions

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter		Min	Typ	Max	Unit
V_I	Input voltage		5.5	-	10	V
T_J	Junction temperature		-40	-	150	°C

9. Electrical characteristics

Over recommended operating free-air temperature range, V_I = 13.5 V, T_J = −40°C to 150°C (unless otherwise noted) (see Figure 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_O	Output voltage	I_O = 200 mA, V_I = 5.5 V to 10 V		4.80	4.85	4.91	V
I_o	Output current			-	-	450	mA
I_q	Current consumption, $I_q = I_I - I_O$	I_O = 1 mA	T_J = 25°C	-	-	510	µA
		I_O = 250 mA		-	6	10	mA
		I_O = 400 mA		-	11	22	mA
V_{DO}	Dropout voltage[4]	I_O = 300 mA, $V_{DO} = V_I - V_O$		-	325	500	mV
	Load regulation	I_O = 5 mA to 400 mA		-	100	200	mV
	Line regulation	ΔV_I = 8 V to 32 V, I_O = 5 mA		-15	5	15	mV
PSRR	Power supply ripple rejection	f_r = 100 Hz, V_r = 0.5 V_{pp}		-	40	-	dB
$V_{O, rt}$	RESET switching threshold			4.4	4.6	4.7	V
V_{ROL}	RESET output low voltage	$R_{ext} \geq 5$ kΩ, $V_O > 1$ V		-	0.2	0.4	V
I_{ROH}	RESET output leakage current	V_{ROH} = 5 V		-	0	10	µA

[1] Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] All voltage values are with respect to the network ground terminal.

[3] The ESD performance of pins CANH, CANL, RTH and RTL, with respect to GND, was verified by an external test house in accordance with IEC-61000-4-2 (C = 150 pF, R = 330 Ω).

[4] Measured when the output voltage V_O has dropped 100 mV from the nominal value obtained at V_I = 13.5 V

$I_{D,c}$	RESET charging current	V_D = 1 V	3	5.5	17	µA
V_{DU}	RESET upper timing threshold		1.5	2.7	4.5	V
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{DRL}	RESET lower timing threshold		0.2	0.4	3.5	V

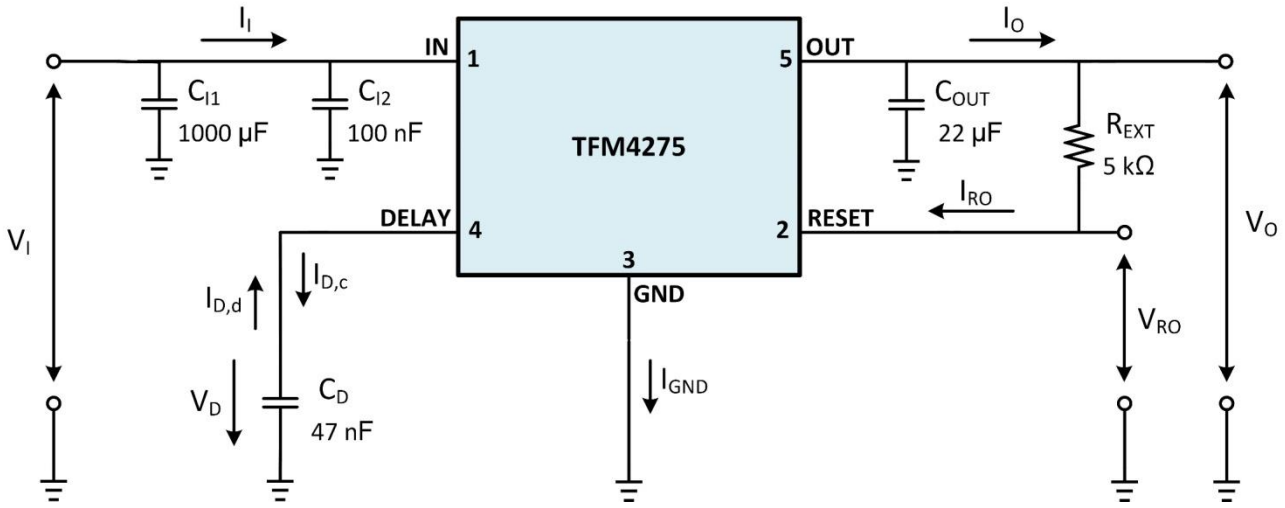


Figure 3: Test circuit

10. Switching characteristics

Over operating free-air temperature range (unless otherwise noted) (see Figure 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rd}	RESET delay time	C_D = 47 nF	10	14	35	ms
t_{rr}	RESET reaction time	C_D = 47 nF	-	1.5	2	µs

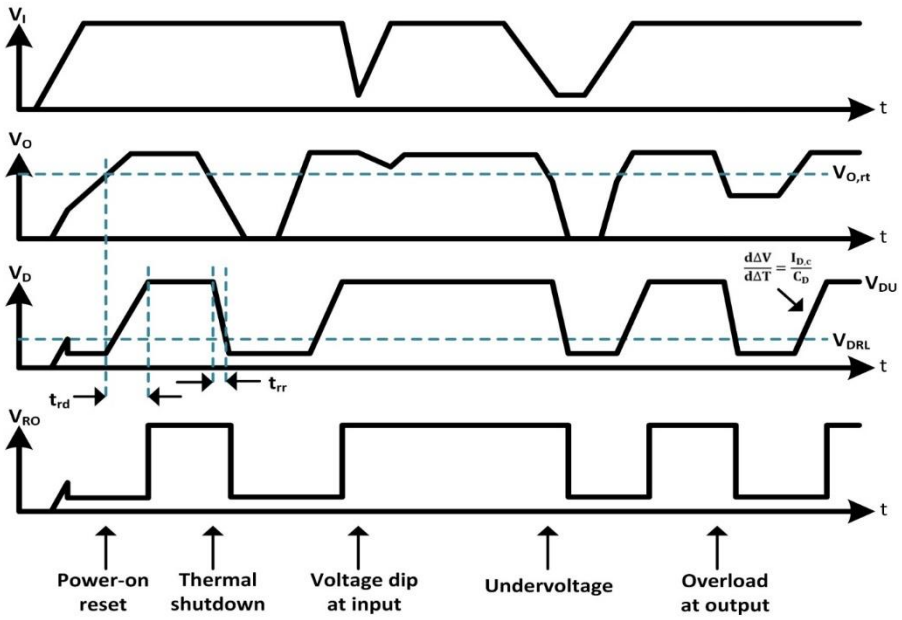


Figure 4: Reset timing diagram

11. Thermal characteristics

Symbol	Thermal metric	5-pin TO-252	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.8	
$R_{\theta JA}$	Junction-to-board thermal resistance	17.2	
Ψ_{JT}	Junction-to-top characterization parameter	2.8	
Ψ_{JB}	Junction-to-board characterization parameter	17.1	
$R_{\theta JC(BOT)}$	Junction-to-case (bottom) thermal resistance	0.7	

12. Typical characteristics

13. Detailed description

13.1 Feature description

13.1.1 Regulated output (OUT)

The OUT terminal is the regulated 5-V output. The output has a current limitation. During initial power up, the regulator has a soft start incorporated to control the initial current through the pass element. If the regulator drops out of regulation, the output tracks the input minus a drop based on the load current.

13.1.2 Power-on-reset (RESET)

The power-on-reset is an output with an external pull-up resistor to the regulated supply. The reset output remains low until the regulated V_O exceeds approximately 4.65 V and the power-on-reset delay has expired.

13.1.3 Reset delay timer

An external capacitor on this terminal sets the timer delay before the reset terminal is asserted high. The constant output current charges an external capacitor until the voltage exceeds a threshold to trip an internal comparator. The reset pulse delay time t_d, is defined with the charge time of an external capacitor DELAY.

$$t_d = \frac{C_{delay} \times V_{DU}}{I_{D,c}}$$

13.2Device functional modes

13.2.1Low-voltage tracking

At low input voltages, the regulator drops out of regulation and the output voltage tracks input minus a voltage based on the load current (I_O) and the switch resistance ($R_{(SW)}$). This allows for a smaller input capacitor and can eliminate the need of using a boost converter during cold-crank conditions.

14. Application and implementation

14.1 Application information

Figure 21 shows typical application circuits for the AS4275. Based on the end application, different values of external components can be used. An application can require a larger output capacitor during fast load steps in order to prevent a reset from occurring. It recommends a low-ESR ceramic capacitor with a dielectric of type X5R or X7R for better load transient response.

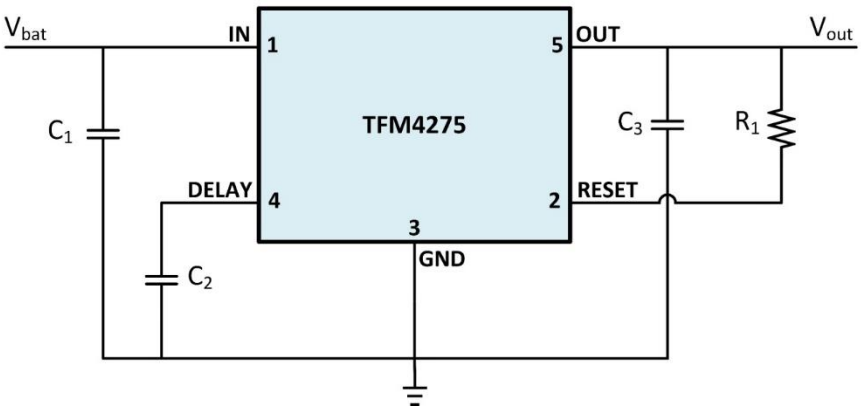


Figure 5: Typical application diagram

14.1.1 Design requirement

For this design example, use the parameters listed in the next table.

Design parameter	Example value
Input voltage range	6 to 40 V
Output voltage	5 V
Output current rating	400 mA
Output capacitor range	10 to 500 µF
Output capacitor ESR range	1 mΩ to 20 Ω
DELAY capacitor range	100 pF to 500 nF

14.1.2 Detailed design procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Input voltage range
- Output capacitor
- Power-up reset delay time

14.1.2.1 Power-up reset capacitance

To calculate the power-up reset capacitance:

$$t_d = \frac{C_{delay} \times V_{DU}}{I_{D,c}}$$

$$C_{delay} = \frac{t_d \times I_{D,c}}{V_{DU}} = \frac{t_d \times 5.5 \times 10^{-6}}{1.8}$$

14.1.2.2 Thermal consideration

Calculate the power dissipated by the device according to:

$$P_T = I_O \times (V_I - V_O) + V_I \times I_Q$$

Where:

- P_T = total power dissipation of the device
- I_o = output current
- V_I = input voltage
- V_O = output voltage

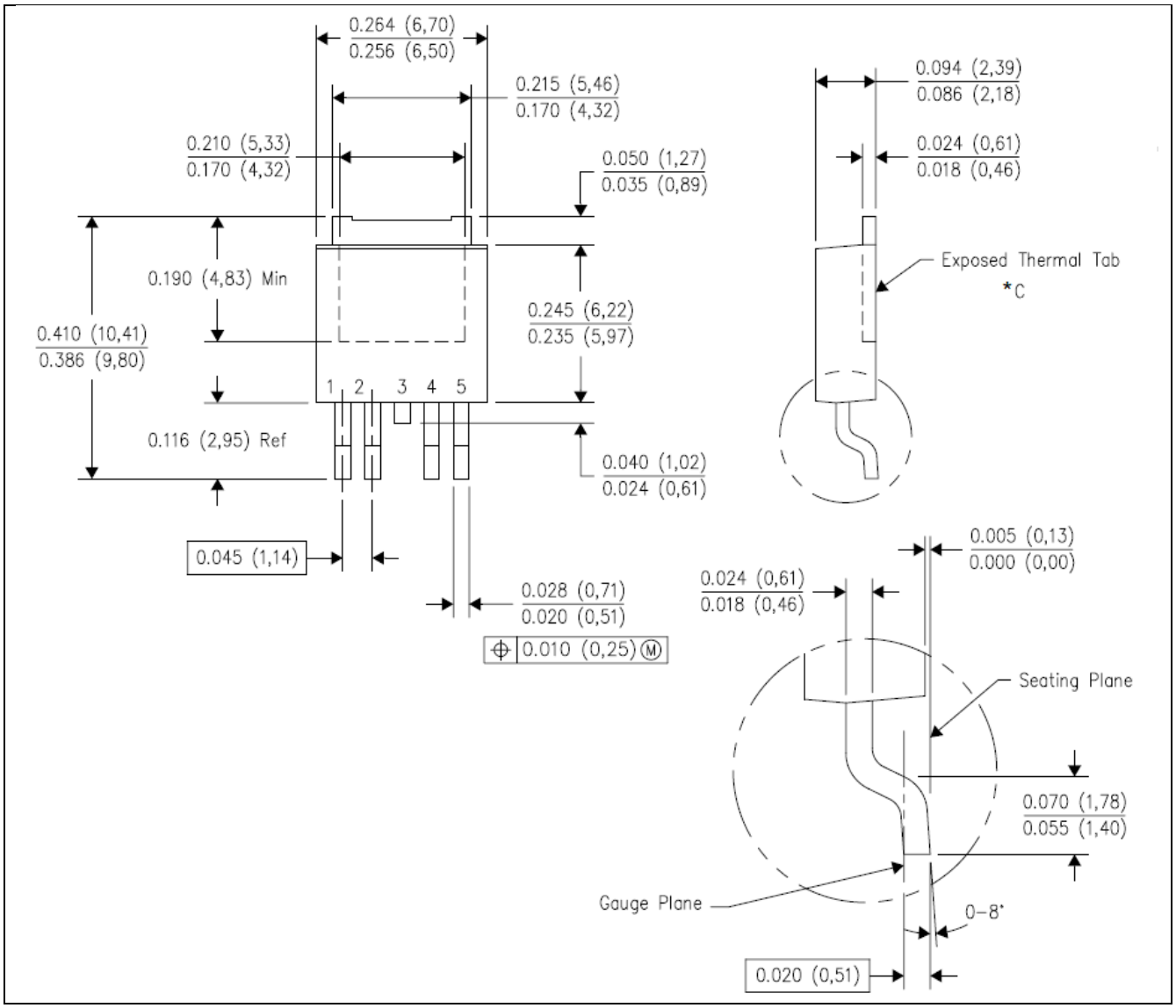
After determining the power dissipated by the device, calculate the junction temperature from the ambient temperature and the device thermal impedance:

$$T_J = T_A + R_{\theta JA} \times P_T$$

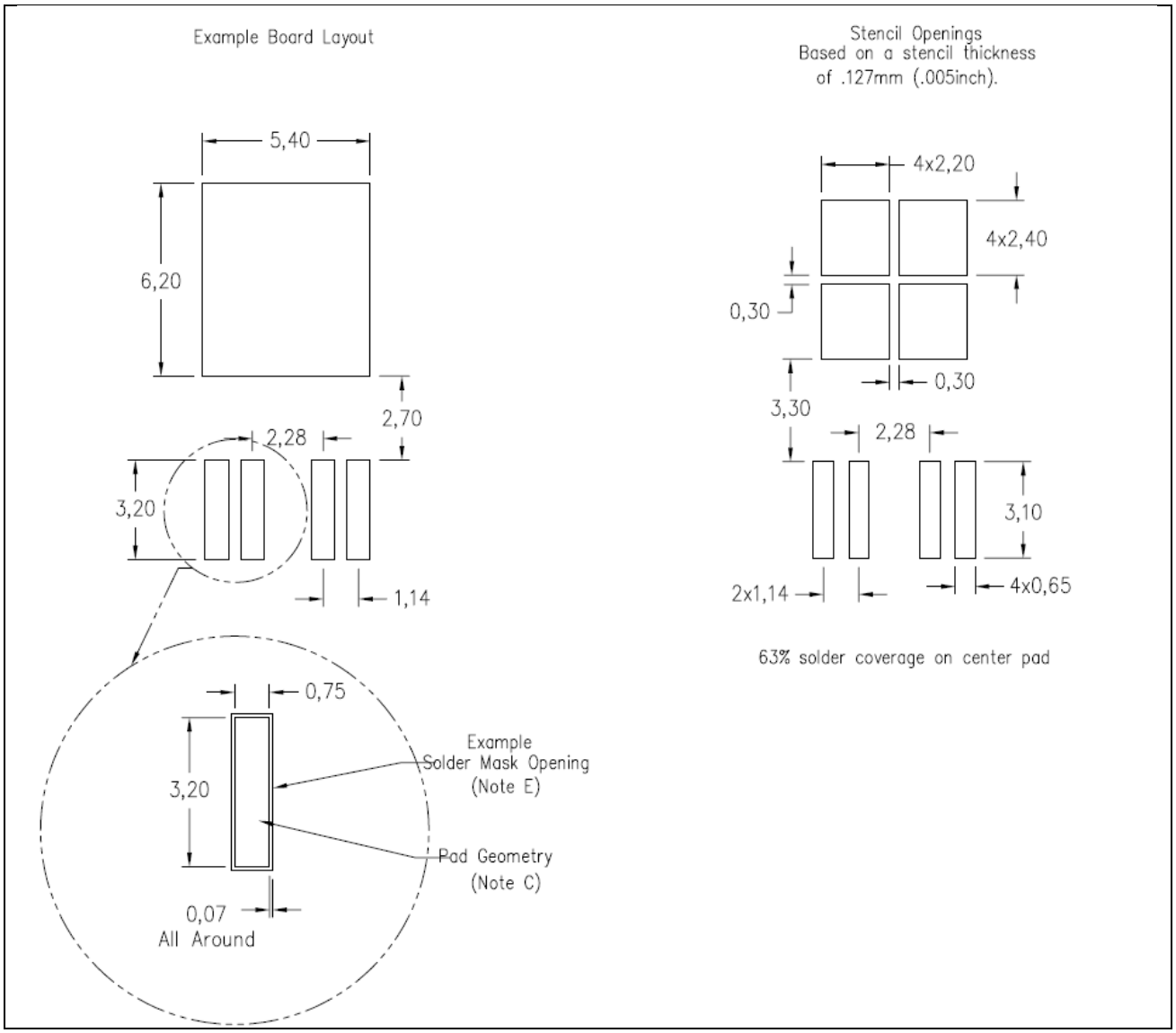
15. Power supply recommendations

The device is designed to operate from an input voltage supply range between 6 V and 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the AS4275 device, an electrolytic capacitor with a value of 47 µF and a ceramic bypass capacitor are recommended to add to the input.

16. Packaging



Notes:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
*C. The center lead is in electrical contact with the exposed thermal tab.
D. Body dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.006 (0.15) per side.
E. Falls within JEDEC TO-252 variation AD.



Notes:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-SM-782 is an alternate information source for PCB land pattern design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pads.