1. Introduction

This transceiver can be used as the interface between the protocol controller and the physical bus wires in a Controller Area Network (CAN). It is primarily intended for low-speed applications up to 125 kBd in passenger cars. The device provides differential receive and transmit capability and will switch to single-wire transmitter and/or receiver in error conditions.

2. Features

2.1 General

- Operating supply range 6 V ≤ V_{BAT} ≤ 26 V
- Baud rates up to 125 kBd
- Up to 32 nodes can be connected
- Supports unshielded bus wires
- Low Electro-Magnetic Emission (EME) and high Electro-Magnetic Immunity (EMI) based on IEC 62228 (2007)
- Fully ISO 11898-3:2006 compliant
- High ESD robustness
- Transmit Data (TXD) dominant time-out function
- High receiver common mode input voltage range at no fault condition
- Low-voltage microcontroller support

2.2 Protections

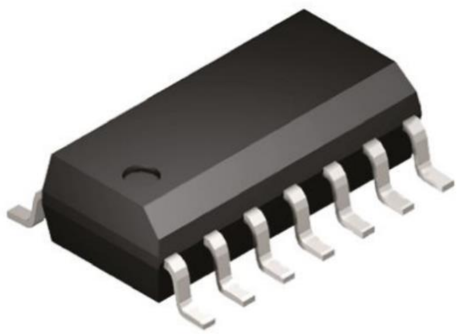
- Over-temperature protection
- Under-voltage protection on V_{CC}
- Battery supply under-voltage protection
- Bus pins short-circuit safe to battery and ground
- Bus lines are protected against transients in an automotive environment
- An unpowered node does not disturb the bus lines
- Microcontroller interface without reverse current paths, if unpowered

2.3 Bus failure management

- Supports single-wire transmission modes with ground offset voltages up to 1.5 V
- Automatic switching to single-wire mode in the event of bus failures, even when the CANH bus wire is short-circuited to V_{CC}
- Automatic reset to differential mode if bus failure is removed
- Full wake-up capability during failure modes

2.4 Low power modes

- Low quiescent current in sleep and standby modes with wake-up via bus lines
- Software accessible power-on reset flag



AS1055
14-PIN SOIC

3. Pin configuration

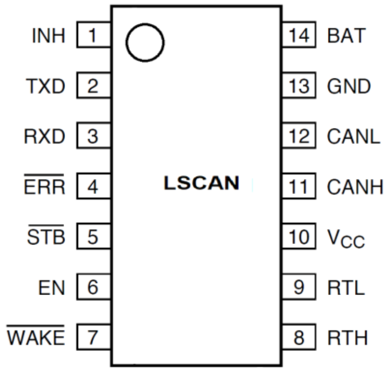


Figure 1: Pin configuration

Symbol	Description
INH	Inhibit output for switching an external voltage regulator if a wake-up signal occurs
TXD	Transmit data input for activating the driver to the bus lines
RXD	Receive data output for reading out the data from the bus lines
$\overline{ERR}$	Error, wake-up, and power-on indication output; active LOW in normal operating mode when a bus failure is detected; active LOW in standby and sleep mode when a wake-up is detected; active LOW in power-on standby when a V_{BAT} power-on event is detected
$\overline{STB}$	Standby digital control signal input; together with the input signal on pin EN this input determines the state of the transceiver
EN	Enable digital control signal input; together with the input signal on pin $\overline{STB}$ this input determines the state of the transceiver
$\overline{WAKE}$	Local wake-up signal input (active low); both falling and rising edges are detected
RTH	Termination resistor connection; in case of a CANH bus wire error the line is terminated with a predefined impedance
RTL	Termination resistor connection; in case of a CANL bus wire error the line is terminated with a predefined impedance
VCC	Supply voltage
CANH	High-level CAN bus line
CANL	Low-level CAN bus line
GND	Ground
BAT	Battery supply voltage

4. Quick reference data

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{BAT}	Battery Supply voltage	No time limit	-0.3	-	40	V
		Operating mode	5.0	-	40	V
		Load dump	-	-	40	V
I_{BAT}	Battery Supply current	Sleep mode at $V_{RTL} = V_{WAKE} = V_{INH} = V_{BAT} = 14$ V; $T_{amb} = -40$°C to +125°C	-	-	82	µA
V_{CC}	Supply voltage		4.75	-	5.25	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CANH}	Voltage on pin CANH	$V_{CC} \geq 0$ V; $V_{BAT} \geq 0$ V; no time limit; with respect to any other pin	-40	-	40	V
V_{CANL}	Voltage on pin CANL	$V_{CC} \geq 0$ V; $V_{BAT} \geq 0$ V; no time limit; with respect to any other pin	-40	-	40	V
$V_{O(dom)}$	Dominant output voltage	$V_{TXD} = 0$ V; $V_{EN} = V_{CC}$				
	On pin CANH	$I_{CANH} = -40$ mA	$V_{CC} - 1.4$	-	-	V
	On pin CANL	$I_{CANL} = 40$ mA	-	-	1.4	V
$t_{pd(L)}$	Propagation delay TXD (low) to RXD (low)	No failures; $R_{CANL} = R_{CANH} = 125\ \Omega$; $C_{CANL} = C_{CANH} = 1$ nF	-	-	1.4	µs
T_{vj}	Virtual junction temperature		-40	-	+150	℃

5. Ordering information

Part number	Package		
	Name	Description	Version
	SO-14	Plastic small outline package; 14 leads; body width 3.9 mm	-

6. Block diagram

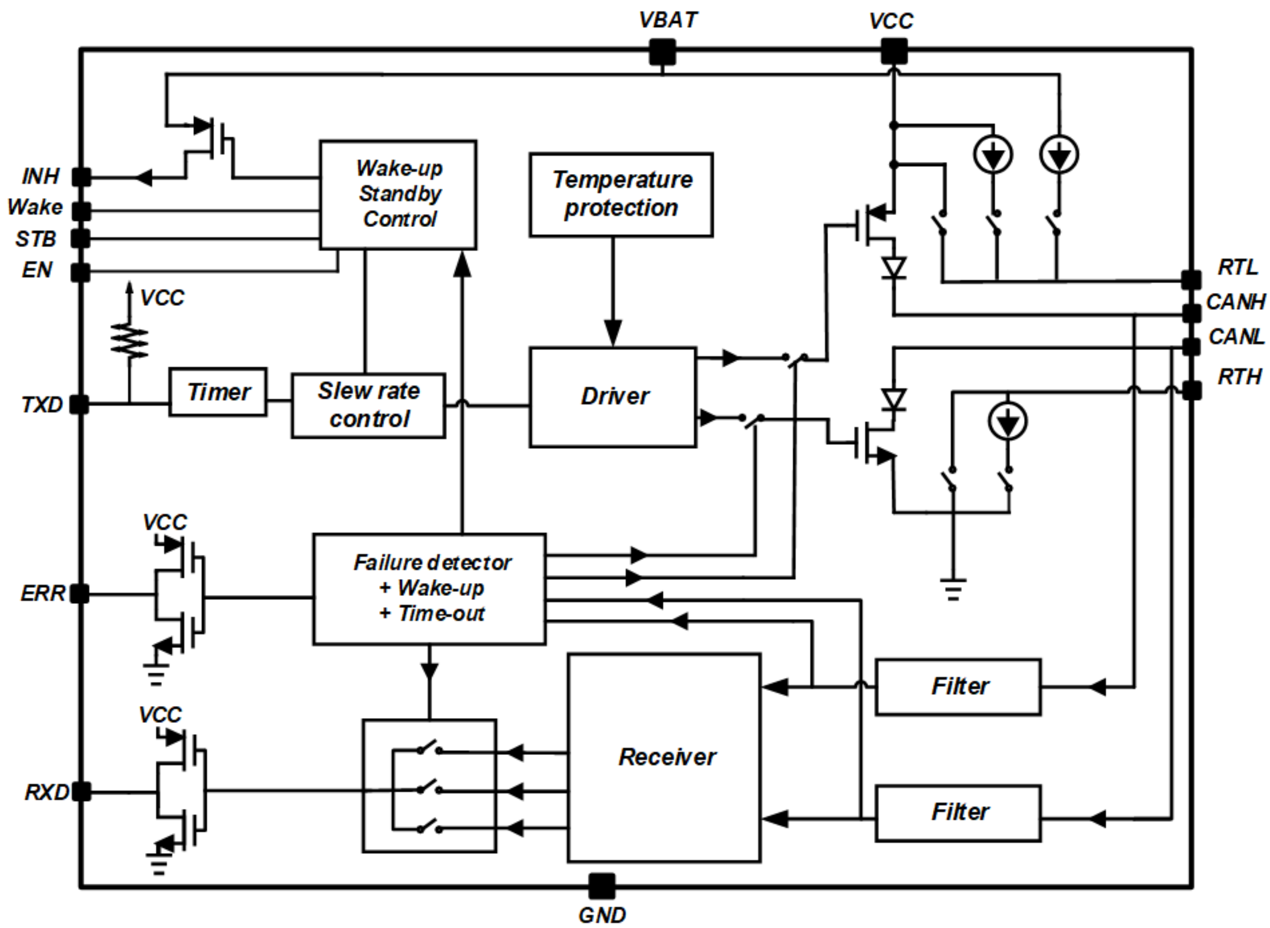


Figure 2: Block diagram

7. Absolute maximum ratings [1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{BAT}	Battery supply voltage		-0.3	+40	V
V_{CC}	Supply voltage		-0.3	+5.5	V
V_{INH}	Voltage on pin INH		-0.3	V_{BAT} + 0.3	V
V_{TXD}	Voltage on pin TXD		-0.3	V_{CC} + 0.3	V
V_{RXD}	Voltage on pin RXD		-0.3	V_{CC} + 0.3	V
V_{ERR}	Voltage on pin $\overline{ERR}$		-0.3	V_{CC} + 0.3	V
V_{STB}	Voltage on pin $\overline{STB}$		-0.3	V_{CC} + 0.3	V
V_{EN}	Voltage on pin EN		-0.3	V_{CC} + 0.3	V
$V_{I(WAKE)}$	Input voltage on pin $\overline{WAKE}$	With respect to any other pin	-0.3	+40	V
$I_{I(WAKE)}$	Input current on pin $\overline{WAKE}$	[2]	-25	-	mA
R_{RTH}	Termination resistance on pin RTH		500	16000	Ω
R_{RTL}	Termination resistance on pin RTL		500	16000	Ω
V_{RTH}	Voltage on pin RTH	With respect to any other pin	-40	40	V
V_{RTL}	Voltage on pin RTH	With respect to any other pin	-40	40	V
V_{CANH}	Voltage on pin CANH	$V_{CC} \geq 0$ V; $V_{BAT} \geq 0$ V; no time limit; with respect to any other pin	-40	+40	V
V_{CANL}	Voltage on pin CANL	$V_{CC} \geq 0$ V; $V_{BAT} \geq 0$ V; no time limit; with respect to any other pin	-40	+40	V
V_{trt}	Transient voltage on pins CANH and CANL	[3]	-120	+80	V
T_{stg}	Storage temperature		-50	+150	℃
T_{vj}	Virtual junction temperature	[4]	-40	+150	℃
V_{esd}	Electrostatic discharge voltage	IEC 61000-4-2[5]			
		Pins RTH, CANH and CANL	-8	+8	kV
		Pin RTL	-5	+7	kV
		All other pins	-4	+4	kV

8. Static characteristics

V_{CC} = 4.75 V to 5.25 V; V_{BAT} = 5.0 V to 40 V; V_{STB} = V_{CC}; T_{vj} = -40 ℃ to +150 ℃; all mentioned voltages are defined with respect to ground; positive currents flow into the device; unless otherwise specified.[6]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin V_{CC}						
V_{BAT}	Battery supply voltage	No time limit	-0.3	-	40	V

[1] In accordance with IEC 60134.

[2] Only relevant if $V_{WAKE} < V_{GND}$ - 0.3 V; current will flow into pin GND.

[3] Test set-up according to IEC TS 62228, section 4.2.4. Verified by an external test house to ensure pins can withstand ISO 7637 part 1 & 2 automotive transient test pulses 1, 2a, 3a and 3b.

[4] Junction temperature in accordance with *"IEC 60747-1"*. An alternative definition is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$ where $R_{th(vj-a)}$ is a fixed value to be use for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and operating ambient temperature (T_{amb}).

[5] The ESD performance of pins CANH, CANL, RTH and RTL, with respect to GND, was verified by an external test house in accordance with IEC-61000-4-2 (C = 150 pF, R = 330 Ω).

[6] All parameters are guaranteed over the virtual junction temperature range by design, but only 100 % tested at T_{amb} = 125℃ for dies on wafer level, and above this for cased products 100 % tested at T_{amb} = 25℃, unless otherwise specified).

		Operating mode	5.0	-	40	V
		Load dump	-	-	40	V
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
I_{BAT}	Battery supply current	Sleep mode at $V_{RTL} = V_{WAKE} = V_{INH} = V_{BAT}$ = 14 V; T_{amb} = -40°C to +125°C	-	-	82	µA
		Low power mode at $V_{RTL} = V_{WAKE} = V_{INH} = V_{BAT}$; T_{amb} = -40°C to +125°C				
		V_{BAT} = 5 V to 8 V	10	-	100	µA
		V_{BAT} = 8 V to 40 V	10	-	115	µA
		Normal operating mode at $V_{RTL} = V_{WAKE} = V_{INH} = V_{BAT}$ = 5 V to 40 V	-	150	220	µA
$V_{pof(BAT)}$	Power-on flag voltage on pin BAT	Low power modes				
		Power-on flag set	-	-	3.8	V
		Power-on flag not set	5	-	-	V
V_{CC}	Supply voltage		4.75	-	5.25	V
$V_{CC\ (stb)}$	Supply voltage for forced standby mode (fail-safe)		3.1	-	4.5	V
I_{CC}	Supply current	Normal operating mode; $V_{TXD} = V_{CC}$ (recessive)	2.5		10	mA
		Normal operating mode; V_{TXD} = 0 V (dominant); no load	3	-	21	mA
		Low power modes at $V_{TXD} = V_{CC}$				
		T_{amb} = -40°C to +85°C	0	0	26	µA
		T_{amb} = +85°C to +125°C	0	0	25	µA
Pins $\overline{STB}$, EN and TXD						
V_{IH}	High-level input voltage		2.2	-	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		- 0.3	-	0.8	V
I_{IH}	High-level input current					
	Pins $\overline{STB}$ and EN	V_I = 4 V	-	45	60	µA
	Pin TXD	V_I = 3 V	-160	-80	-40	µA
I_{IL}	Low-level input current					
	Pins $\overline{STB}$ and EN	V_I = 1 V	2	11	-	µA
	Pin TXD	V_I = 1 V	-400	-180	-100	µA
Pins RXD and $\overline{ERR}$						
$V_{OH\ (norm)}$	High-level output voltage in normal mode					
	On pin $\overline{ERR}$	I_O = -100 µA	V_{CC} - 0.9	-	V_{CC}	V
	On pin RXD	I_O = -1 mA	V_{CC} - 0.9	-	V_{CC}	V
$V_{OH\ (lp)}$	High-level output voltage in low-power mode					
	On pin $\overline{ERR}$	I_O = -100 µA	V_{CC} - 1.1	V_{CC} - 0.7	V_{CC}-0.4	V
	On pin RXD	I_O = -100 µA	V_{CC} - 1.1	V_{CC} - 0.7	V_{CC}-0.4	V
V_{OL}	Low-level output voltage	I_O = -1.6 mA	0	-	0.4	V
		I_O = -1.2 mA; $V_{CC} < 4.75$ V	0	-	0.4	V
		I_O = -5 mA	0	-	1.5	V
Pin INH						
ΔV_H	High-level voltage drop	I_{INH} = -0.18 mA; $V_{BAT} \geq 5.5$ V	-	-	0.8	V
		I_{INH} = -0.18 mA; $V_{BAT} = 5$ V	-	-	1.0	V

$\lvert I_L \rvert$	Leakage current	Sleep mode; V_{INH} = 0 V	-	-	5	µA
Pin $\overline{WAKE}$						
I_{IL}	Low-level input current	V_{WAKE} = 0 V; V_{BAT} = 40 V	-12	-1	0	µA
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
$V_{th(wake)}$	Wake-up threshold voltage	V_{STB} = 0 V	2.5	3.2	3.9	V
Bus lines; pins CANH and CANL						
$V_{th(dif)}$	Differential receiver threshold voltage	No failures and bus failures 1, 2, 5, and 6a; (See Figure 3)				
		V_{CC} = 5 V	-3.5	-3.2	-2.9	V
		V_{CC} = 4.75 V to 5.25 V	-0.70V_{CC}	-0.64V_{CC}	-0.58V_{CC}	V
$V_{O\ (dom)}$	Dominant output voltage	V_{TXD} = 0; V_{EN} = V_{CC}				
	On pin CANH	I_{CANH} = -40 kA	V_{CC} – 1.75	-	-	V
	On pin CANL	I_{CANL} = 40 kA	-	-	1.4	V
$V_{O\ (reces)}$	Recessive output voltage	V_{TXD} = V_{CC}				
	On pin CANH	R_{RTH} < 4 kΩ	-	-	0.2	V
	On pin CANL	R_{RTL} < 4 kΩ	V_{CC} - 0.2	-	-	V
$I_{O(CANH)}$	Output current on pin CANH	Normal mode; V_{CANH} = 0 V; V_{TXD} = 0 V	-110	-80	-45	mA
		Low power modes; V_{CANH} = 0 V; V_{CC} = 5 V	-	-0.25	-	µA
$I_{O(CANL)}$	Output current on pin CANL	Normal mode; V_{CANL} = 14 V; V_{TXD} = 0 V	45	70	100	mA
		Normal mode; V_{CANL} = 14 V; V_{BAT} = 14 V	-	0	-	µA
$V_{det(sc)(CANH)}$	Detection voltage for short-circuit to battery voltage on pin CANH	Normal mode; V_{CC} = 5 V	1.5	1.7	1.85	V
		Low power modes	1.1	1.8	2.5	V
$V_{det(sc)(CANL)}$	Detection voltage for short-circuit to battery voltage on pin CANL	Normal mode				
		V_{CC} = 5 V	6.6	7.2	7.8	V
		V_{CC} = 4.75 V to 5.25 V	1.32V_{CC}	1.44V_{CC}	1.56V_{CC}	V
$V_{th(wake)}$	Wake-up threshold voltage					
	On pin CANH	Low power modes	1.5	1.8	2.5	V
	On pin CANL	Low power modes	2.5	3.2	3.9	V
$\Delta V_{th(wake)}$	Difference of wake-up threshold voltages on CANL and CANH	Low power modes	0.8	1.4	-	V
$V_{th(se)(CANH)}$	Single-ended receiver threshold voltage on pin CANH	Normal operating mode and failures 4, 6 and 7				
		V_{CC} = 5 V	1.5	1.7	1.85	V
		V_{CC} = 4.75 V to 5.25 V	0.30V_{CC}	0.34V_{CC}	0.37V_{CC}	V
$V_{th(se)(CANL)}$	Single-ended receiver threshold voltage on pin CANL	Normal operating mode and failures 3 and 3a				
		V_{CC} = 5 V	3.11	3.3	3.45	V
		V_{CC} = 4.75 V to 5.25 V	0.62V_{CC}	0.66V_{CC}	0.69V_{CC}	V
$R_{i(dif)}$	Differential input resistance	Normal mode	220	330	540	kΩ
$R_{i(se)(CANH)}$	Single-ended input resistance on pin CANH	Normal mode	110	165	270	kΩ
$R_{i(se)(CANL)}$	Single-ended input resistance on pin CANL	Normal mode	110	165	270	kΩ
Pins RTH and RTL						

$R_{sw\,(RTH)}$	Switch-on resistance on pin RTH	Normal operating mode; switch-on resistance between pin RTH and GND; $\lvert I_O \rvert$ < 10 mA	-	40	100	Ω
$R_{sw\,(RTL)}$	Switch-on resistance on pin RTL	Normal operating mode; switch-on resistance between pin RTL and GND; $\lvert I_O \rvert$ < 10 mA	-	40	100	Ω
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
$V_{O(RTH)}$	Output voltage on pin RTH	Low power modes; I_O = 100 µA	-	0.7	1.0	V
$I_{O(RTL)}$	Output current on pin RTL	Low power modes; V_{RTL} = 0 V	-1.5	-0.65	0	mA
$I_{pu\,(RTL)}$	Pull-up current on pin RTL	Normal operating mode and failures 4, 6 and 7	-	60	-	µA
$I_{pd\,(RTH)}$	Pull-down current on pin RTH	Normal operating mode and failures 3 and 3a	-	75	-	µA
Thermal shutdown						
$T_{j(sd)}$	Shut down junction temperature		160	170	190	°C

9. Dynamic characteristics

V_{CC} = 4.75 V to 5.25 V; V_{BAT} = 5.0 V to 40 V; V_{STB} = V_{CC}; T_{vj} = -40 °C to +150 °C; R_{CANH} = R_{CANL} = 125 Ω; C_{CANH}=C_{CANL}= 1 nF; all mentioned voltages are defined with respect to ground; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{t(r-d)}$	Transition time for recessive to dominant (on pins CANL and CANH)	Between 10 % and 90 %; (See Figure 5)	0.2	-	-	µs
$t_{t(d-r)}$	Transition time for dominant to recessive (on pins CANL and CANH)	Between 10 % and 90 %; (See Figure 5)	0.2	-	-	µs
$t_{pd(low)}$	Propagation delay TXD (low) to RXD (low)	No failures; (See Figure 3 and Figure 5)	-	-	1.5	µs
		All failures except CANL shorted to CANH; (See Figure 3 and Figure 5)	-	-	1.9	µs
		failure 7, CANL shorted to CANH; R_{CANL}=1 MΩ; (See Figure 3 and Figure 5)	-	-	1.9	µs
$t_{pd(high)}$	Propagation delay TXD (high) to RXD (high)	No failures; (See Figure 3 and Figure 5)	-	-	1.5	µs
		All failures except CANL shorted to CANH; (See Figure 3 and Figure 5)	-	-	1.9	µs
		failure 7, CANL shorted to CANH; R_{CANL}=1 MΩ; (See Figure 3 and Figure 5)	-	-	1.9	µs
$t_{dis(TXD)}$	Disable time of TXD permanent dominant timer	Normal mode; V_{TXD} = 0 V	0.75	-	4	ms
t_{WAKE}	Local wake-up time on pin $\overline{ERR}$	Low power modes; V_{BAT} = 14 V; for wake-up after receiving a falling or rising edge	7	-	38[2]	µs

[1] All parameters are guaranteed over the virtual junction temperature range by design, but only 100 % tested at T_{amb} = 125°C for dies on wafer level, and above this for cased products 100 % tested at T_{amb} = 25°C, unless otherwise specified.
[2] To guarantee a successful mode transition under all conditions, the maximum specified time must be applied.

$t_{dom(CANH)}$	Dominant time on pin CANH	Low power modes; V_{BAT} = 14 V	7	-	38[2]	µs
$t_{dom(CANL)}$	Dominant time on pin CANL	Low power modes; V_{BAT} = 14 V	7	-	38[2]	µs
t_{det}	Failure detection time	Normal operating mode				
		Failures 3 and 3a	0.9	-	8.0	ms
		Failures 4, 6 and 7	0.3	-	1.6	ms
		Low power modes; V_{BAT} = 14 V				
		Failures 3 and 3a	1.6	-	8.0	ms
		Failures 4 and 7	0.1	-	1.6	ms
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
n_{det}	Pulse-count failure detection	Difference between CANH and CANL; normal operating mode and failures 1, 2, 5, and 6a; pin $\overline{ERR}$ becomes low	-	4	-	
t_{rec}	Failure recovery time	Normal operating mode				
		Failures 3 and 3a	0.3	-	1.6	ms
		Failures 4 and 7	7	-	38	µs
		Failure 6	125	-	750	µs
		Low power modes; V_{BAT} = 14 V				
		Failure 3, 3a, 4 and 7	0.3	-	1.6	ms
n_{rec}	Number of consecutive pulses for failure recovery	On CANH and CANL simultaneously; failures 1, 2, 5 and 6a	-	4	-	

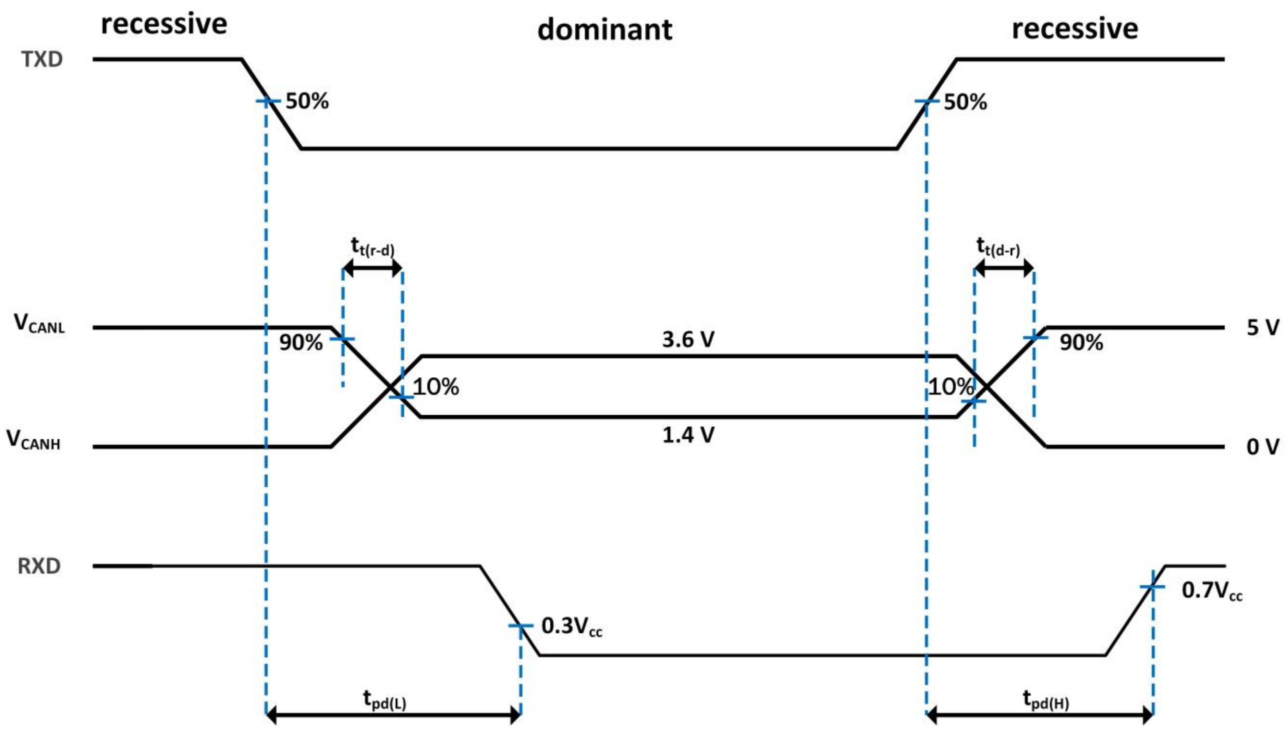


Figure 3: Timing diagram

10. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	Thermal resistance from junction to ambient	In free air	150	K/W
$R_{th(j-s)}$	Thermal resistance from junction to substrate	In free air	50	K/W

11. Functional description

The LSCAN can be used as the interface between the protocol controller and the physical bus wires in a Controller Area Network (CAN). It is primarily intended for low-speed applications up to 125 kBd in passenger cars. The device provides differential transmit capability to the CAN bus and differential receive capability to the CAN controller.

In normal operating mode, the differential receiver is output on pin RXD. The differential receiver inputs are connected to pins CANH and CANL through integrated filters. The filtered input signals are also used for the single-wire receivers. The receivers connected to pins CANH and CANL have threshold voltages that ensure a maximum noise margin in single-wire mode. A timer function (TXD dominant time-out function) has been integrated to prevent the bus lines from being driven into a permanent dominant state (thus blocking the entire network communication) due to a situation in which pin TXD is permanently forced to a low level, caused by any application failure.

If the duration of the low level on pin TXD exceeds a certain time, the transmitter will be disabled. The timer will be reset by a high level on pin TXD.

To reduce EME, the rise and fall slopes are limited. This allows the use of an unshielded twisted pair or a parallel pair of wires for the bus lines.

The device supports transmission capability on either bus line if one of the wires is corrupted. The failure detection logic automatically selects a suitable transmission mode.

11.1 Failure detector

The failure detector is fully active in the normal operating mode. After the detection of a single bus failure the detector switches to the appropriate mode. The differential receiver threshold voltage is set at -3.2 V typical with respect to V_{CC}=5V. This ensures correct reception with a noise margin as high as possible in the normal operating mode and the event of failures 1, 2, 5, and 6a.

These failures, or recovery from them, do not destroy ongoing transmissions. The output drivers remain active, the termination does not change and the receiver remains in differential mode.

Failures 3, 3a, and 6 are detected by comparators connected to the CANH and CANL bus lines. Failures 3 and 3a are detected in a two-step approach. If the CANH bus line exceeds a certain voltage level, the differential comparator signals a continuous dominant condition. After a first time-out, the transceiver switches to single-wire operation through CANH. If the CANH bus line is still exceeding the CANH detection voltage for a second time-out, it switches to CANL operation; the CANH driver is switched off and the RTH bias changes to the pull-down current source. The time-outs (delays) are needed to avoid false triggering by external RF fields.

Failure 6 is detected if the CANL bus line exceeds its comparator threshold for a certain period of time. This delay is needed to avoid false triggering by external RF fields. After detection of failure 6, the reception is switched to the single-wire mode through CANH; the CANL driver is switched off and the RTL bias changes to the pull-up current source.

Recovery from failures 3, 3a, and 6 are detected automatically after reading a consecutive recessive level by corresponding comparators for a certain period of time.

Failures 4 and 7 initially result in a permanent dominant level on pin RXD. After a time-out, the CANL driver is switched off and the RTL bias changes to the pull-up current source. Reception continues by switching to the single-wire mode via pins CANH or CANL. When failures 4 or 7 are removed, the recessive bus levels are restored. If the differential voltage remains below the recessive threshold level for a certain period of time, reception and transmission switch back to the differential mode.

If any wiring failure occurs, the output signal on pin $\overline{\mathrm{ERR}}$ will be set to low. On error recovery, the output signal on pin $\overline{\mathrm{ERR}}$ will be set to high again. In case of an interrupted open bus wire, this failure will be detected and signaled only if there is an open wire between the transmitting and receiving node(s). Thus, during open wire failures, pin $\overline{\mathrm{ERR}}$ typically toggles.

During all single-wire transmissions, EMC (electromagnetic compatibility) performance (both immunity and emission) is worse than in the differential mode. The integrated receiver filters suppress any HF noise induced into the bus wires. The cut-off frequency of these filters is a compromise between propagation delay and HF suppression. In single-wire mode, LF noise cannot be distinguished from the required signal.

Failure	Description	RTH	RTL	CANH driver	CANL driver	Receiver mode
1	CANH wire interrupted	on	on	on	on	Differential
2	CANL wire interrupted	on	on	on	on	Differential
3	CANH short-circuited to battery	weak[1]	on	off	on	CANL
3a	CANH short-circuited to V_{CC}	weak[1]	on	off	on	CANL
4	CANL short-circuited to ground	on	weak[2]	on	off	CANH
5	CANH short-circuited to ground	on	on	on	on	Differential
6	CANL short-circuited to battery	on	weak[2]	on	off	CANH
6a	CANL short-circuited to V_{CC}	on	on	on	on	Differential
7	CANL and CANH mutually short-circuited	on	weak[2]	on	off	CANH

11.2 Low power modes

The LSCAN transceiver provides three low power modes (sleep, standby, and power-on standby) which can be entered and exited via $\overline{\mathrm{STB}}$ and EN (Figure 4).

The sleep mode is the mode with the lowest power consumption. Pin INH is switched to high-impedance for deactivation of the external voltage regulator. Pin CANL is biased to the battery voltage via pin RTL. Pins RXD and $\overline{\mathrm{ERR}}$ will signal the wake-up interrupt even in case V_{CC} is not present.

The standby mode operates in the same way as the sleep mode but with a high level on pin INH.

[1] This implies a pull-down current source behavior of 75 µA typical.
[2] This implies a pull-up current source behavior of 75 µA typical.

The power-on standby mode is the same as the standby mode, however, in this mode, the battery power-on flag is shown on pin ERR instead of the wake-up interrupt signal. The output on pin RXD will show the wake-up interrupt. This mode is only for reading out the power-on flag.

The following table describes mentioned low power modes and normal operating mode.

Mode	Pin $\overline{STB}$	Pin EN	Pin $\overline{ERR}$		Pin RXD		Pin RTL switched to
			LOW	HIGH	LOW	HIGH	
Go to sleep command	Low	High	wake-up interrupt signal[1]	[2]	wake-up interrupt signal[2]	[3]	V_{BAT}
Sleep	Low	Low[3]					
Stand by	Low	Low					
Power-on standby	High	Low	V_{BAT} power-on flag[4]		wake-up interrupt signal[2]		V_{BAT}
Normal operating	High	High	Error flag	No error flag	dominant received data	recessive received data	V_{CC}

Wake-up requests are recognized by the transceiver through two possible channels:

- The bus lines for remote wake-up
- Pin $\overline{WAKE}$ for local wake-up

In order to wake up the transceiver remotely through the bus lines, a filter mechanism is integrated. This mechanism makes sure that noise and any present bus failure conditions do not result in an erroneous wake-up. Because of this mechanism, it is not sufficient to simply pull the CANH or CANL bus lines to a dominant level for a certain time. To guarantee a successful remote wake-up under all conditions, a message frame with a dominant phase of at least the maximum specified $t_{dom(CANH)}$ or $t_{dom(CANL)}$ in it's required.

A local wake-up through pin $\overline{WAKE}$ is detected by a rising or falling edge with a consecutive level exceeding the maximum specified t_{WAKE}. On a wake-up request, the transceiver will set the output on pin INH to HIGH which can be used to activate the external supply voltage regulator. A wake-up request is signaled on $\overline{ERR}$ or RXD with an active low signal. So, the external microcontroller can activate the transceiver via pins $\overline{STB}$ and EN.

To prevent a false remote wake-up due to transients or RF fields, the wake-up voltage levels have to be maintained for a certain period of time. In the low power modes, the failure detection circuit remains partly active to prevent an increased power consumption in the event of failures 3, 3a, 4, and 7.

To prevent a false local wake-up during an open wire at pin $\overline{WAKE}$, this pin has a weak pull-up current source towards V_{BAT}. However, to protect the transceiver against any EMC immunity issues, it is recommended to connect a not used pin $\overline{WAKE}$ to pin BAT. Pin INH is set to floating only if the go-to sleep command is entered successfully. To enter a successful go-to sleep command under

[1] Wake-up interrupts are released when entering normal operating mode.

[2] For LSCAN a diode is added in series with the high-side driver of $\overline{ERR}$ and RXD to prevent a reverse current from $\overline{ERR}$ to V_{CC} in the unpowered state

[3] In case the go to sleep command was used before. When V_{CC} drops, pin EN will become low, but due to the fail-safe functionality this does not affect the internal functions.

[4] V_{BAT} power-on flag will be reset when entering normal operating mode.

all conditions, this command must be kept stable for the maximum specified $t_{d(sleep)}$.

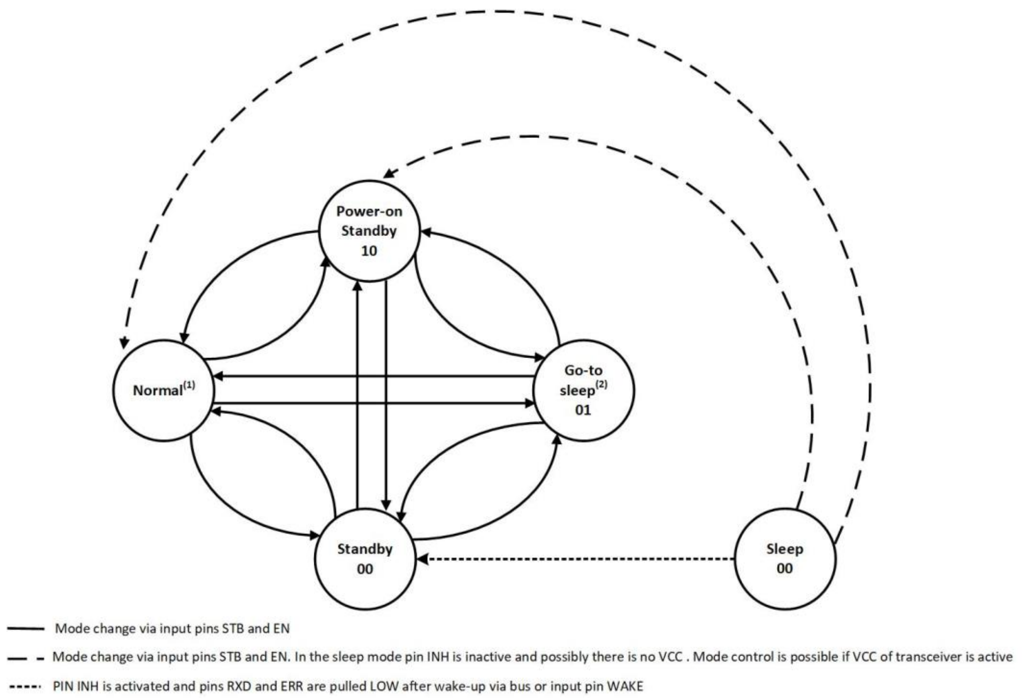
Pin INH will be set to a high level again by the following events only:

- V_{BAT} power-on (cold start)
- Rising or falling edge on pin $\overline{WAKE}$
- Pin $\overline{STB}$ goes to a high level with V_{CC} active
- A message frame with a dominant phase of at least the maximum specified $t_{dom(CANH)}$ or $t_{dom(CANL)}$, while pin EN or pin $\overline{STB}$ is at a low level

To provide fail-safe functionality, the signals on pins $\overline{STB}$ and EN will internally be set to low when V_{CC} is below a certain threshold voltage ($V_{CC\,(stb)}$). An unused output pin INH can simply be left open within the application.

11.3 Power on

After power-on (V_{BAT} switched on) the signal on pin INH will become high and an internal power-on flag will be set. This flag can be read in the power-on standby mode through pin $\overline{ERR}$ ($\overline{STB}$ = 1; EN = 0) and will be reset by entering the normal operating mode.



Mode 01 stands for: Pin $\overline{STB}$ = low and pin EN = high.
(1) Transitions to normal mode clear the internal wake-up: wake-up interrupt flag and power-on flag are cleared.
(2) Transitions to sleep mode: pin INH is deactivated.

Figure 4: Mode control

11.4 Protections

A current limiting circuit protects the transmitter output stages against short-circuit to positive and negative battery voltage.
If the junction temperature exceeds the typical value of 175°C, the transmitter output stages are disabled. Because the transmitter is responsible for the major part of the power dissipation, this will result in a reduced power dissipation and hence a lower chip temperature. All other parts of the device will continue to operate.
The pins CANH and CANL are protected against electrical transients which may occur in an automotive environment.

12. Test information

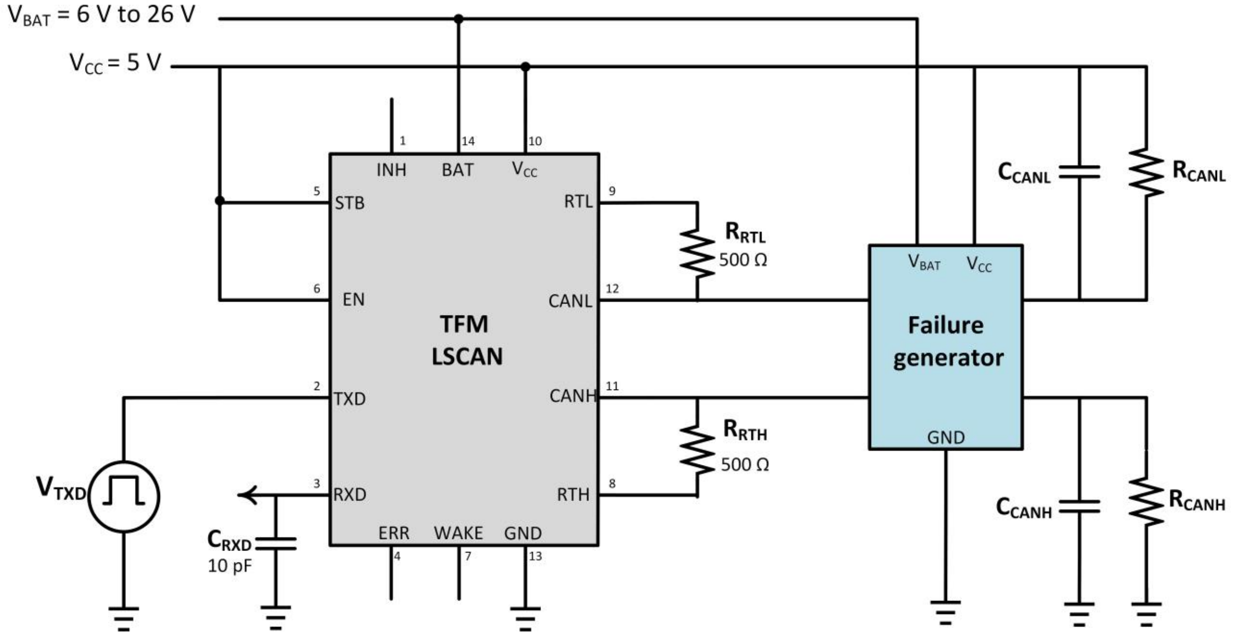


Figure 5: Test circuit for dynamic characteristics

In the test circuit for dynamic characteristics, V_{TXD} is a rectangular signal of 50 kHz with a 50% duty cycle and slope time < 10 ns. Termination resistors R_{CANL} and R_{CANH} (125 Ω) are not connected to pin RTL or pin RTH for testing purposes because the minimum load allowed on the CAN bus lines is 500 Ω per transceiver.

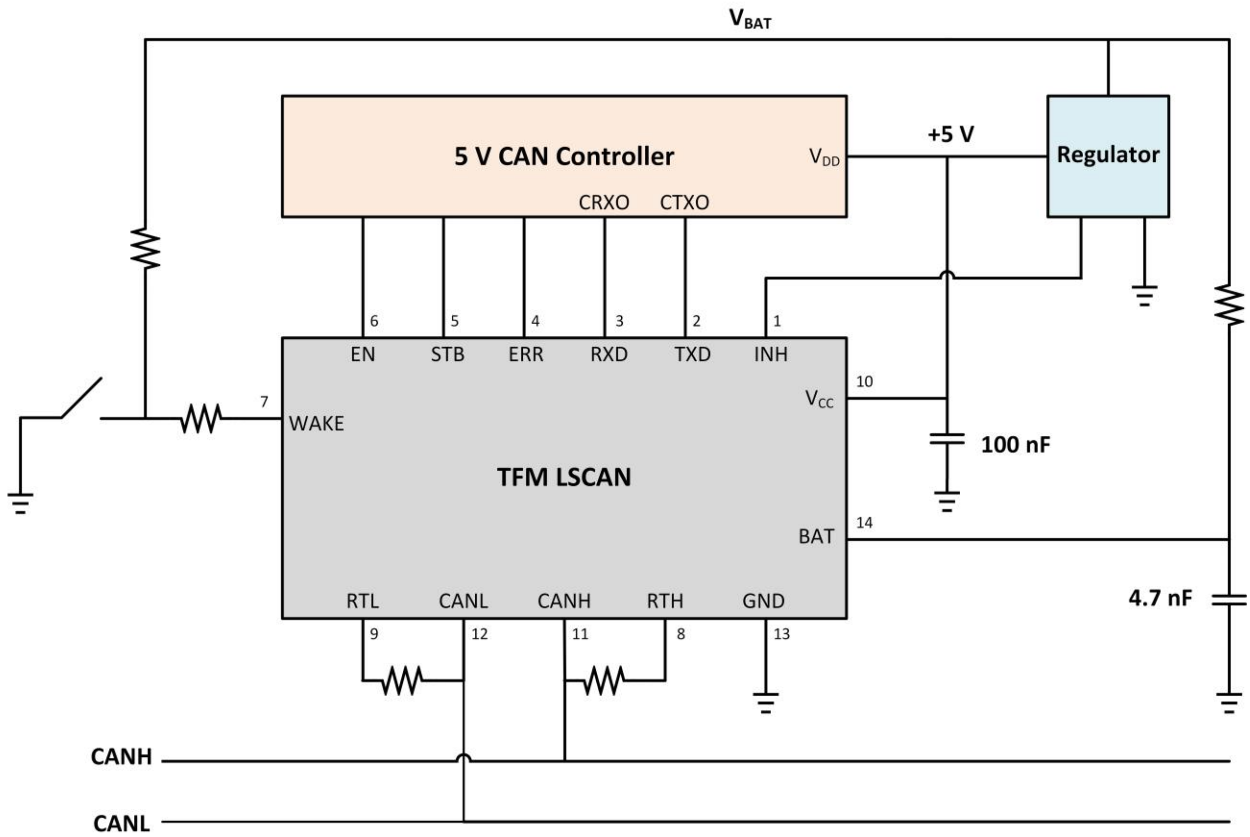


Figure 6: Application diagram

13. Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-G - Failure mechanism-based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

14. Packaging

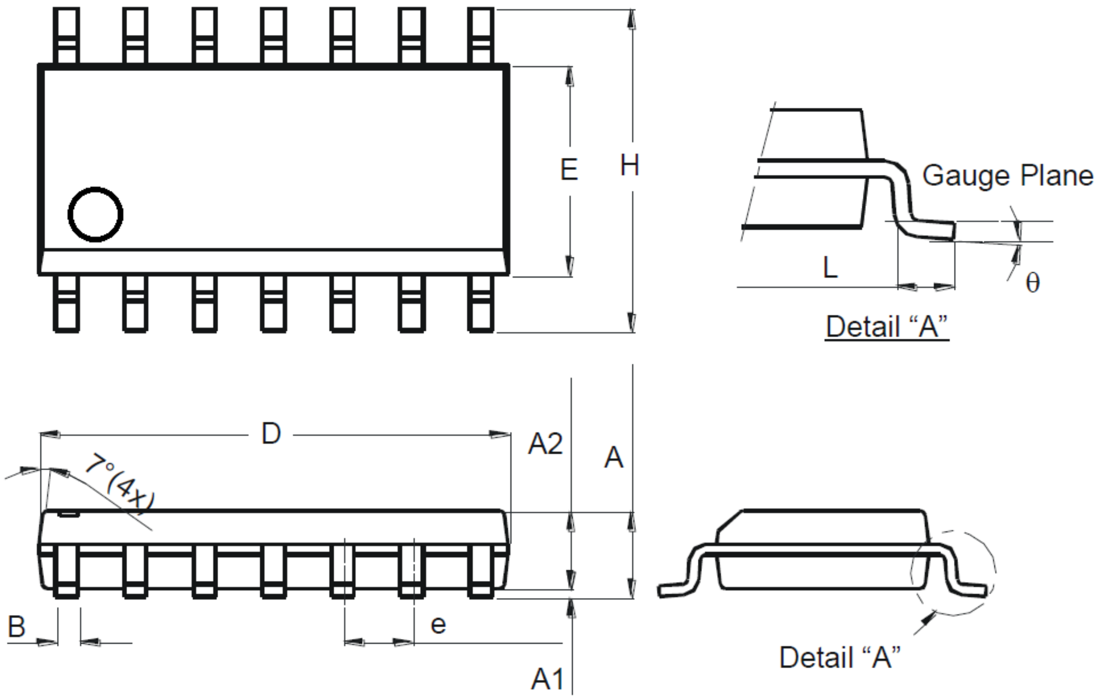


Figure 7: SO14 package outline

Dimensions	Min	Typ	Max	Unit
A	1.47	-	1.73	mm
A1	0.10	-	0.25	mm
A2	-	1.45	-	mm
B	0.33	-	0.51	mm
D	8.53	-	8.74	mm
E	3.80	-	3.99	mm
e	-	1.27	-	mm
H	5.80	-	6.20	mm
L	0.38	-	1.27	mm
θ	0°	-	8°	