1. Introduction

The AS1042 high-speed CAN transceiver provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed CAN applications in the automotive industry, providing the differential transmit and receive capability to (a microcontroller with) a CAN protocol controller. It offers good Electro-Magnetic Compatibility (EMC) and Electro-Static Discharge (ESD) performance.

This CAN transceiver meets the ISO 11898-2:2016 and ISO 11898-5:2007 high speed CAN (Controller Area Network) physical layer standard. The transceiver has a low power standby mode with wake-up capability. Additionally, includes protection feature to enhance device and network robustness.

2. Features

2.1 General

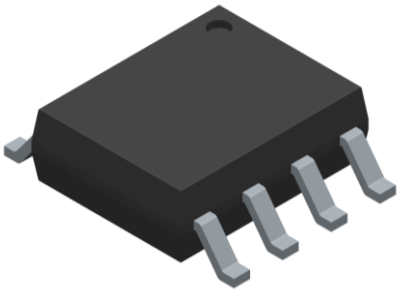
- SPLIT voltage output for stabilizing the recessive bus level
- Low Electro-Magnetic Emission (EME) and high Electro-Magnetic Interference (EMI) immunity based on IEC 62228 (2007)
- Suitable for 12 V systems
- Timing guaranteed for data rates up to 5Mbit/s
- Fully ISO 11898-2:2016 and ISO 11898-5:2007 compliant
- Available in SO8 package
- Dark green product (halogen-free and Restriction of Hazardous Substances (RoHS) compliant)

2.2 Fail-safe behavior

- Low quiescent current in standby mode
- Wake-up capability
- Under-voltage protection on V_{CC}
- Functional behavior predictable under all supply conditions
- Transmit data (TXD) dominant time-out function
- Bus-dominant time-out function in standby-mode
- Transceiver disengages from the bus when not powered up (zero load)

2.3 Protections

- High ESD handling capability on the bus pins (±8 kV)
- Bus pins protected against transients in automotive environments
- Receiver common mode input voltage: ±40 V
- Over temperature protection
- Compatible with TJA1042



AS1042
8-PIN SOIC

3. Pin configuration

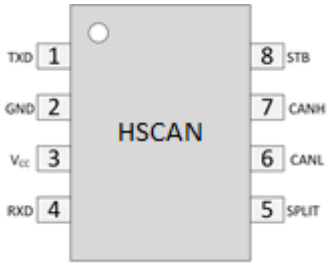


Figure 1: Pin configuration

Symbol	Description
TXD	Transmit data input
GND	Ground
V_{CC}	Supply voltage
RXD	Receive data output; reads out data from the bus lines
SPLIT	Common-mode stabilization output
CANL	Low-level CAN bus line
CALH	High-level CAN bus line
STB	Standby mode control input

4. Quick Reference

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CANH}	Voltage on pin CANH		-40		+40	V
V_{CANL}	Voltage on pin CANL		-40		+40	V
V_{SPLIT}	Voltage on pin SPLIT		-40		+40	V
V_{ESD}	Electrostatic discharge voltage	IEC 61000-4-2 at pins CANH, CANL	-8		+8	KV
V_{CC}	Supply voltage		4.5		5.5	V
I_{CC}	Supply current	Standby mode	15	25	44	µA
		Normal mode: bus recessive	2.5	5	10	mA
		Normal mode: bus dominant	20	45	70	mA
T_{vj}	Virtual junction temperature		-40		+150	°C
$V_{TX,RX,STB}$	Logic voltage		-0.3		V_{CC} + 0.3	V
$V_{uvd(VCC)}$	Undervoltage detection on pin V_{CC}		3.5		4.5	V
$V_{th(POR)}$	Power-on reset threshold voltage		1.3		2.7	V

5. Ordering information

Part number	Package		
	Name	Description	Version
AS1042	SO-8	Plastic small outline package; 8 leads; body width 3.9 mm	-

6. Block Diagram

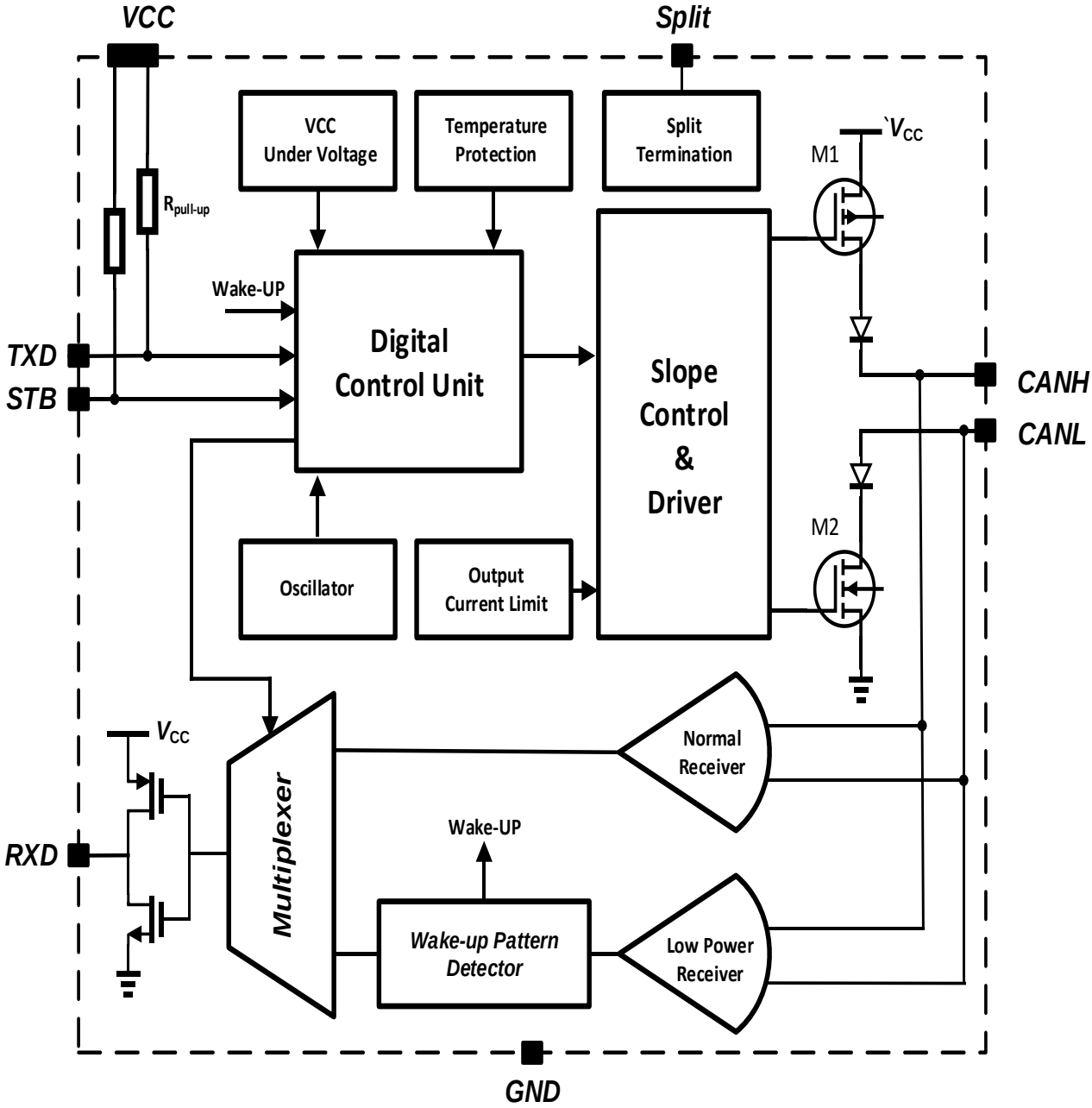


Figure 2: Block diagram

7. Absolute maximum ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_x	Voltage on pin x[1]	on pins CANH, CANL, and SPLIT	-40	+40	V
V_x	Voltage on pin x	on pins TXD, RXD and STB	-0.3	V_{CC} + 0.3	V
V_{diff}	Differential voltage between pin CANH and pin CANL		-27	27	V
V_{trt}	Transient voltage	on pins CANH, CANL[2]			
		pulse 1	-100	-	V
		pulse 2a	-	75	V
		pulse 3a	-150	-	V
		pulse 3b	-	100	V
V_{ESD}	Electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω) [3]			
		at pins CANH and CANL	-8	+8	kV
		at STB pin	-2	+2	kV
		at any other pin	-4	+4	kV
T_{vj}	Virtual junction temperature[4]		-40	+150	°C
V_{CC}	Supply voltage		-0.3	5.5	V

8. Static characteristics

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; R_L = 60 Ω unless specified otherwise; All voltages are defined with respect to ground; Positive currents flow into the IC.[5]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin V_{CC}						
V_{CC}	Supply voltage		4.5	-	5.5	V
$V_{uvd(VCC)}$	Undervoltage detection voltage on pin V_{CC}		3.5	-	4.5	V
$V_{th(POR)}$	Power on reset threshold voltage		1.3	-	2.7	V
I_{CC}	Supply current	Standby mode				
		V_{TXD} = V_{CC}	15	25	44	µA
		Normal mode				
		Recessive; V_{TXD} = V_{CC}	2.5	5	10	mA
		Dominant; V_{TXD} = 0V	20	45	70	mA
		Dominant; V_{TXD} = 0 V; short circuit on bus lines; -3 V < (V_{CANH}=V_{CANL}) < 18 V	2.5	80	110	mA
Standby mode control input; pin STB						
V_{IH}	High-level input voltage		0.7 V_{CC}	-	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		- 0.3	-	0.3 V_{CC}	V

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values
[2]According to IEC TS 62228 (2007), Section 4.2.4; parameters for standard pulses defined in ISO7637 part 2: 2004-06.
[3]According to IEC TS 62228 (2007), Section 4.3; DIN EN 61000-4-2.
[4]In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$ where $R_{th(vj-a)}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).
[5] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IH}	High-level input current	V_{STB} = V_{CC}	-1	-	1	µA
I_{IL}	Low-level input current	V_{STB} = 0 V	-90	-	-1	µA
CAN transmit data input; pin TXD						
V_{IH}	High-level input voltage		0.7 V_{CC}	-	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		- 0.3	-	0.3 V_{CC}	V
I_{IH}	High-level input current	V_{STB} = V_{CC}	-5	-	+5	µA
I_{IL}	Low-level input current	V_{TXD} = 0 V	-260	-150	-30	µA
C_i[6]	Input capacitance		-	2	10	pF
CAN receive data output; pin RXD						
I_{OH}	High-level output current	V_{RXD} = V_{CC} - 0.4 V	-8	-3	-1	mA
I_{OL}	Low-level output current	V_{RXD} = 0.4 V; bus dominant	2	5	12	mA
Bus lines; pins CANH and CANL						
$V_{O(dom)}$	Dominant output voltage	V_{TXD} =0 V; t < $t_{to(dom)TXD}$				
		pin CANH; R_L = 50 Ω to 65 Ω	2.75	3.5	4.5	V
		pin CANL; R_L = 50 Ω to 65 Ω	0.5	1.5	2.25	V
$V_{dom(TX)sym}$	Transmitter dominant voltage symmetry	$V_{dom(TX)sym}$ = V_{CC} -V_{CANH} - V_{CANL}	-400	-	+400	mV
V_{TXsym}	Transmitter voltage symmetry	V_{TXsym} = V_{CANH} + V_{CANL}; [2] f_{TXD} = 250 kHz, 1 MHz and 2.5 MHz; C_{SPLIT} = 4.7 nF; V_{CC} = 4.75 V to 5.25 V[7]	0.9V_{CC}	-	1.1V_{CC}	V
$V_{O(diff)}$	Differential output voltage	Dominant: Normal mode; V_{TXD} = 0 V; t < $t_{to(dom)TXD}$; V_{CC} = 4.75 V to 5.25 V				
		R_L = 45Ω to 65Ω	1.5	-	3	V
		R_L = 45Ω to 70Ω	1.5	-	3.3	V
		R_L = 2240Ω	1.5	-	5	V
		Recessive; no load				
		Normal mode: V_{TXD} = V_{CC}; no load	-50	-	+50	mV
		Standby mode	-0.2	-	0.2	V
$V_{O(rec)}$	Recessive output voltage	Normal mode; V_{TXD} = V_{CC} ; no load	2	0.5V_{CC}	3	V
		Standby mode; no load	-0.1		+0.1	V
$V_{th(RX)diff}$	Differential receiver threshold voltage	-30 V ≤ V_{CANL} ≤ +30 V -30 V ≤ V_{CANH} ≤ +30 V				
		Normal mode	0.5	0.7	0.9	V
		Standby mode	0.4	0.7	1.15	V
$V_{rec(RX)}$	Receiver recessive voltage	-30 V ≤ V_{CANL} ≤ +30 V -30 V ≤ V_{CANH} ≤ +30 V				
		Normal mode;	-4	-	0.5	V
		Standby mode;	-4	-	0.4	V
$V_{dom(RX)}$	Receiver dominant voltage	-30 V ≤ V_{CANL} ≤ +30 V -30 V ≤ V_{CANH} ≤ +30 V				
		Normal mode;	0.9	-	9.0	V
		Standby mode;	1.15	-	9	V
$V_{hys(RX)diff}$	Differential receiver hysteresis voltage	-30 V ≤ V_{CANL} ≤ +30 V -30 V ≤ V_{CANH} ≤ +30 V	50	120	200	mV
$I_{O(sc)dom}$	Dominant short-circuit output current	V_{TXD} =0 V; t < $t_{to(dom)TXD}$; V_{CC} = 5 V				
		pin CANH; V_{CANH} = -3V to +40V	-100	-70	5	mA

[6] Calculated by design

[7] The test circuit used to measure the bus output voltage symmetry (which includes CSPLIT) is shown in Figure 9.

		pin CANL; V_{CANL} = -3V to +40V	-5	70	100	mA
$I_{O(sc)rec}$	Recessive short-circuit output current	Normal mode; $V_{TXD} = V_{CC}$ $V_{CANH} = V_{CANL}$= -27 to 32 V	-5	-	+5	mA
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
I_L	Leakage current	V_{CC} = 0 V or V_{CC} = shorted to ground via 47 kΩ ; $V_{CANH} = V_{CANL}$ = 5 V	-10	-	+10	µA
R_i	Input resistance		9	15	28	kΩ
R_i	Input resistance deviation	Between V_{CANH} and V_{CANL}	-1	-	+1	%
$R_{i(dif)}$	Differential input resistance		19	30	52	kΩ
$C_{i(cm)}$[8]	Common-mode input capacitance		-	-	25	pF
$C_{i(diff)}$[1]	Differential input capacitance		-	-	20	pF
Common mode stabilization output; pin SPLIT						
V_O	Output voltage	Normal mode I_{SPLIT} = -500 µA to +500 µA	$0.3V_{CC}$	$0.5V_{CC}$	$0.7V_{CC}$	V
		Normal mode; R_L =1 MΩ	$0.45V_{CC}$	$0.5V_{CC}$	$0.55V_{CC}$	V
I_L	Leakage current	Standby mode V_{SPLIT} = -12 V to +12 V	-30	-	30	µA
Temperature detection						
$T_{j(sd)}$[1]	Shutdown junction temperature		-	190	-	°C

9. Dynamic characteristic

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; R_L = 60 Ω unless specified otherwise; All voltages are defined with respect to ground; Positive currents flow into the IC.[9]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Transceiver timing; pins CANH, CANL, TXD, and RXD; see figure 5 and figure 6						
$t_{d(TXD-busdom)}$	Delay time from TXD to bus dominant	Normal mode	-	65	-	ns
$t_{d(TXD-busrec)}$	Delay time from TXD to bus recessive	Normal mode	-	90	-	ns
$t_{d(busdom-RXD)}$	Delay time from bus dominant to RXD	Normal mode	-	100	-	ns
$t_{d(busrec-RXD)}$	Delay time from bus recessive to RXD	Normal mode	-	50	-	ns
$t_{d(TXDL-RXDL)}$	Delay time from TXD LOW to RXD LOW	Normal mode	60	-	220	ns
$t_{d(TXDH-RXDH)}$	Delay time from TXD HIGH to RXD HIGH	Normal mode	60	-	220	ns
$t_{bit(bus)}$	Transmitted recessive bit width	$t_{bit(TXD)}$ = 500 ns[10]	435	-	530	ns
$t_{bit(RXD)}$	Bit time on pin RXD	$t_{bit(TXD)}$ = 500 ns[2]	400	-	550	ns
Δt_{rec}	Receiver timing symmetry	$t_{bit(TXD)}$ = 500 ns	-65	-	+40	ns
$t_{to(dom)TXD}$	TXD dominant time-out time	V_{TXD} = 0 V; Normal mode	0.3	2	5	ms
$t_{to(dom)bus}$	Bus dominant time-out time	Standby mode	0.3	2	5	ms
$t_{fltr(wake)bus}$	Bus wake-up filter time	Standby mode	0.5	1	3	µs
$t_{d(stb-norm)}$	Standby to normal mode delay time		7	25	47	µs

[8] Calculated by design

[9] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[10] See figure 7

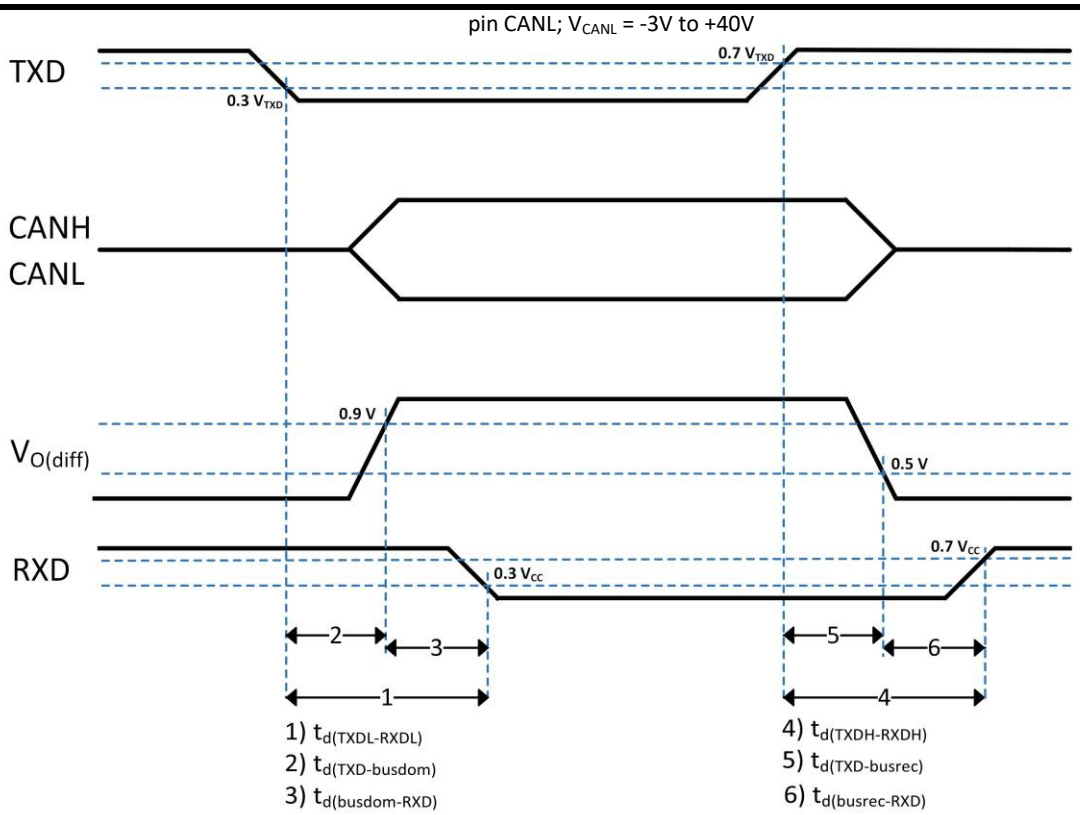


Figure 3: Timing diagram

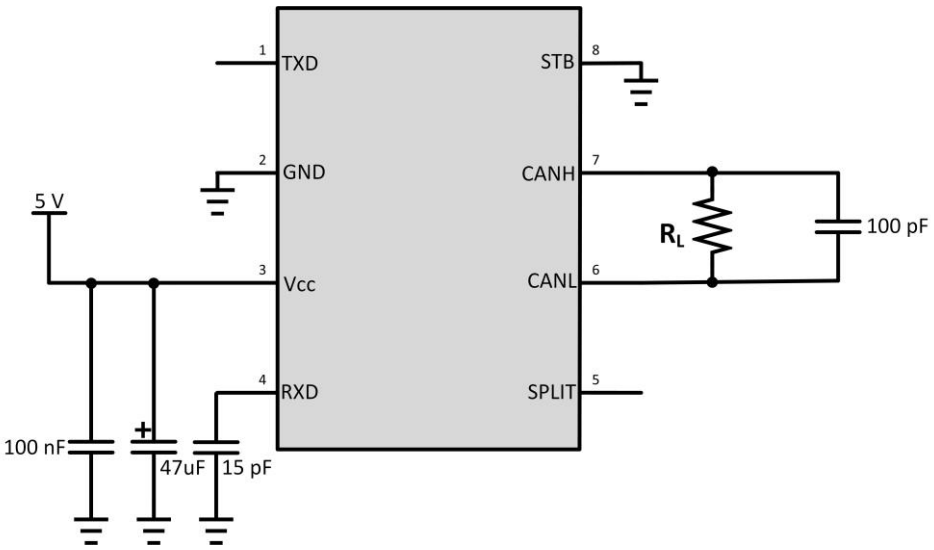
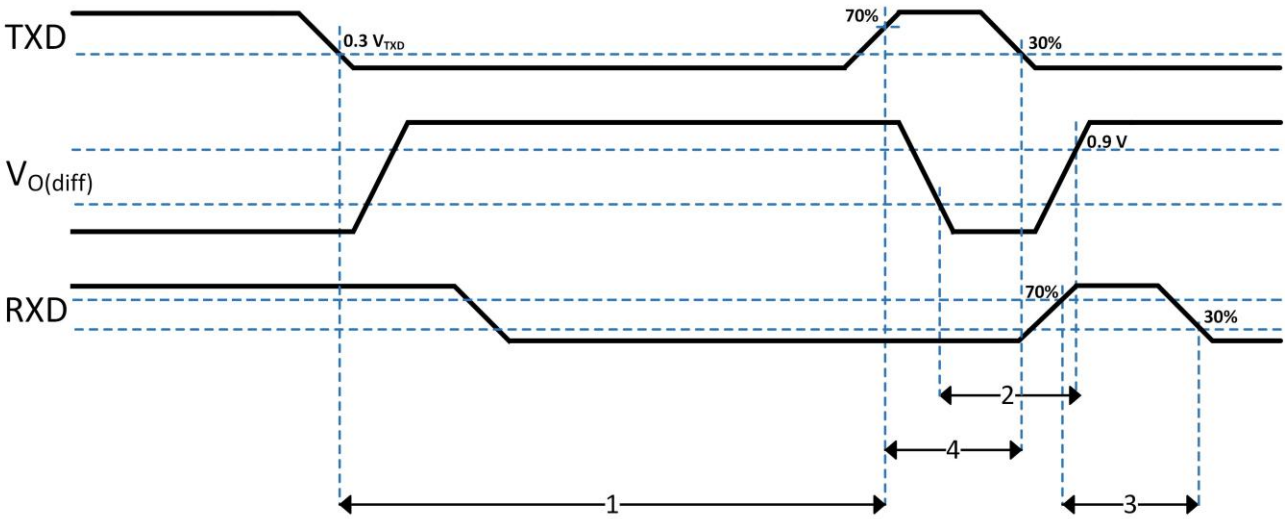


Figure 4: Timing test circuit



1) 5X $t_{bit(TXD)}$
2) $t_{bit(bus)}$
3) $t_{bit(RXD)}$
4) $t_{bit(TXD)}$

Figure 5: Loop delay symmetry

10. Thermal characteristics

Symbol	Parameter	Condition	Value	Unit
$R_{th(vj-a)}$ [11]	Thermal resistance from virtual junction to ambient	SO8 package; in free air	145	K/W

11. Test information

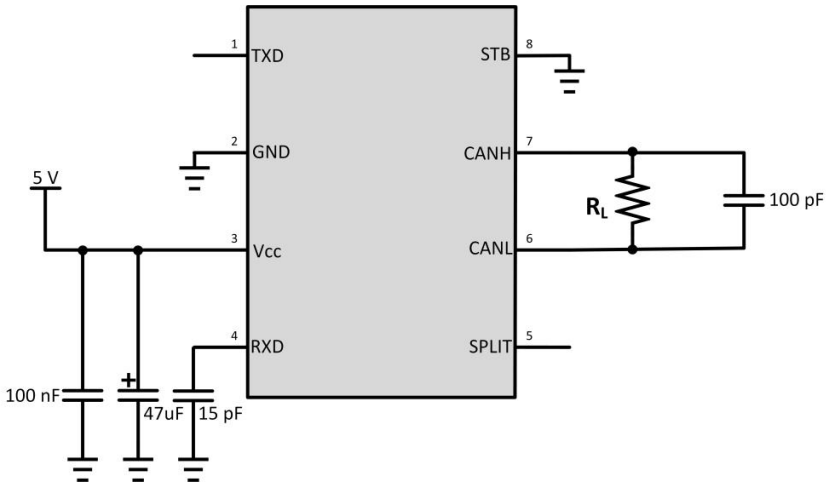


Figure 6: timing test circuit

[11] According to IEC 60747-1

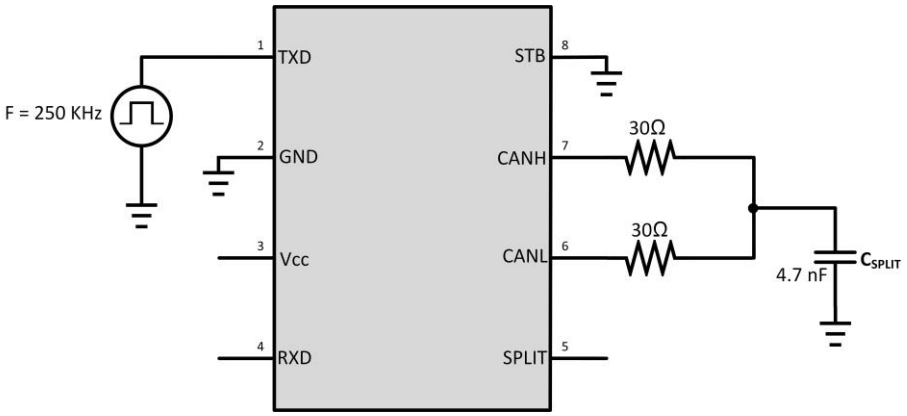


Figure 7: Test circuit for measuring transceiver drive symmetry

12. Functional Description

12.1 Operating mode

The transceiver supports two operating modes, Normal and Standby, which are selected via pin STB. See this table for a description of the operating modes under normal supply conditions.

Mode	Pin STB	Pin RXD	
		LOW	HIGH
Normal	LOW	Bus dominant	Bus recessive
Standby	HIGH	Wake-up request detected	No Wake-up request detected

12.1.1 Normal mode

A LOW level on pin STB selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines CANH and CANL (see Figure 2 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME.

12.1.2 Standby mode

A HIGH level on pin STB selects Standby mode. In Standby mode, the transceiver is not able to transmit or correctly receive data via the bus lines. The transmitter and Normal-mode receiver blocks are switched off to reduce supply current, and only a low-power differential receiver monitors the bus lines for activity. The wake-up filter on the output of the low-power receiver does not latch bus dominant states but ensures that only bus dominant and bus recessive states that persist longer than $t_{filtr(wake)bus}$ are reflected on pin RXD.

In Standby mode, the bus lines are biased to the ground to minimize the system supply current. When pin RXD goes LOW to signal a wake-up request, a transition to Normal mode will not be triggered until STB is forced LOW.

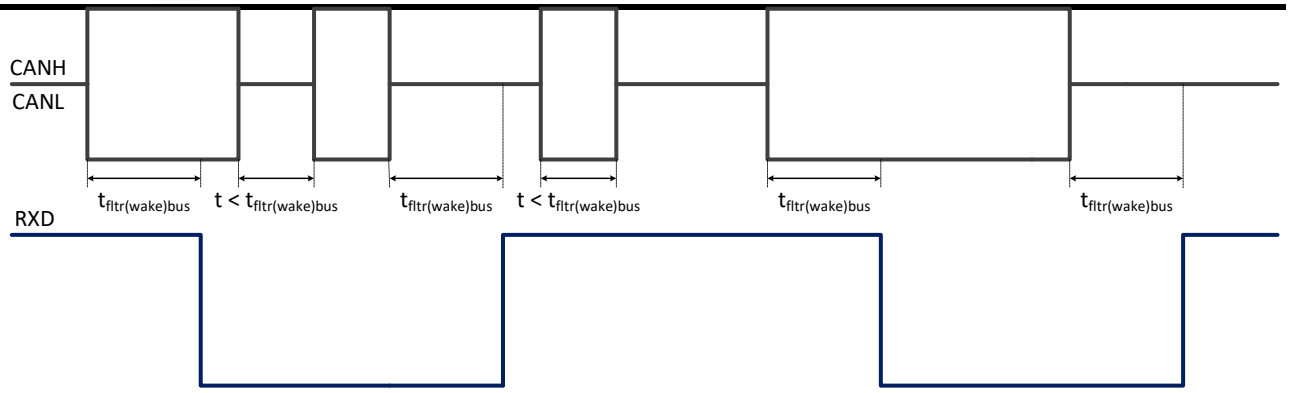


Figure 8: Wake-up timing

12.2 Fail-Safe Features

12.2.1 TXD dominant time-out function

A "TXD dominant time-out" timer is started when pin TXD is set LOW. If the LOW state on pin TXD persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD is set to HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 40 Kbit/s.

12.2.2 Bus dominant time-out function

In Standby mode, a "bus dominant time-out" timer is started when the CAN bus changes from recessive to dominant state. If the dominant state on the bus persists for longer than $t_{to(dom)bus}$, the RXD pin is reset to HIGH. This function prevents a clamped dominant bus (due to a bus short-circuit or a failure in one of the other nodes on the network) from generating a permanent wake-up request. The bus dominant time-out timer is reset when the CAN bus changes from dominant to recessive state.

12.2.3 Undervoltage detection on pin VCC and POR threshold

Should V_{CC} drop below the V_{CC} undervoltage detection level, $V_{uvd(VCC)}$, the transceiver will switch to Standby mode. The logic state of pin STB will be ignored until VCC has recovered.

If V_{cc} drops below the $V_{th(POR)}$ the transceiver will switch off and disengage from the bus (zero load) until V_{cc} has recovered.

12.2.4 Overtemperature protection

The output drivers are protected against overtemperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature, $T_{j(sd)}$, the output drivers will be disabled until the virtual junction temperature falls below $T_{j(sd)}$ and TXD becomes recessive again. Including the TXD condition ensures that output driver oscillation due to temperature drift is avoided.

12.3 Split pin

Using the SPLIT pin in conjunction with a split termination network (see Figure 4 and Figure 10) can help to stabilize the recessive voltage level on the bus. This will reduce EME in networks with DC leakage to ground (e.g. from deactivated nodes with poor bus leakage performance). In Normal mode, pin SPLIT delivers a DC output voltage of $0.5V_{CC}$. In Standby mode or when V_{CC} is off, pin SPLIT is floating. When not used, the SPLIT pin should be left open.

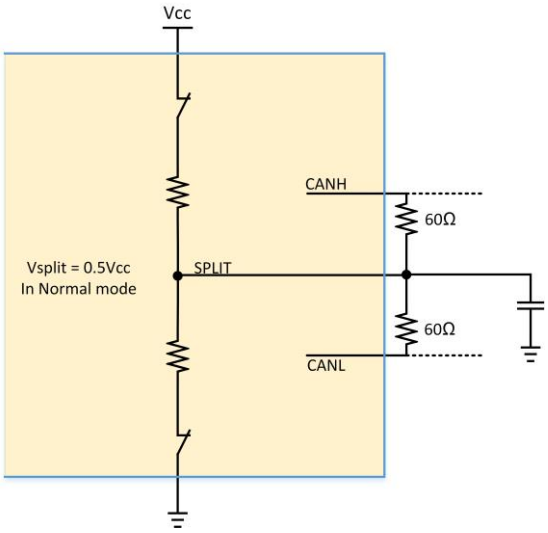


Figure 9: Stabilization circuitry and application

13. Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q100 Rev-G - Failure mechanism-based stress test qualification for integrated circuits and is suitable for use in automotive applications.

14. Application information

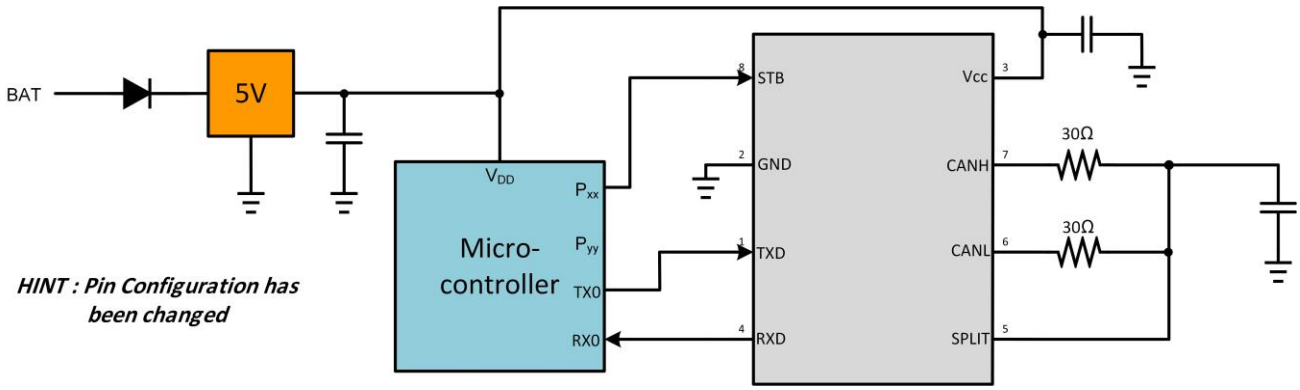


Figure 10: Typical application with a 5V microcontroller

15. Packaging

15.1 Summary

Terminal position code	D (double)
Package type descriptive code	SO8
Package type industry code	SO8
Package style descriptive code	SO (small outline)
Package body material type	P (plastic)
Mounting method type	S (surface mount)

Symbol	Parameter	Min	Nom	Max	Unit
A	Seated height		1.75	1.75	mm
A_2	Package height	1.25	1.35	1.45	mm
D	Package length	4.8	4.9	5	mm
e	Nominal pitch		1.27		mm
E	Package width	3.8	3.9	4	mm
n_2	Actual quantity of termination		8		

15.2 Package outline

Parameter	Min	Max	Unit
D[*]	4.8	5	mm
y	0.1	0.1	mm

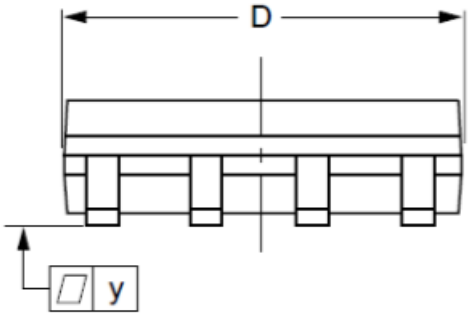


Figure 11

Parameter	Min	Max	Unit
A_{MAX}	1.75	1.75	mm
A_1	0.1	0.25	mm
A_2	1.25	1.45	mm
A_3	0.25	0.25	mm
L	1.05	1.05	mm
L_p	0.4	1.0	mm
Q	0.6	0.7	mm
θ	0°	8°	mm

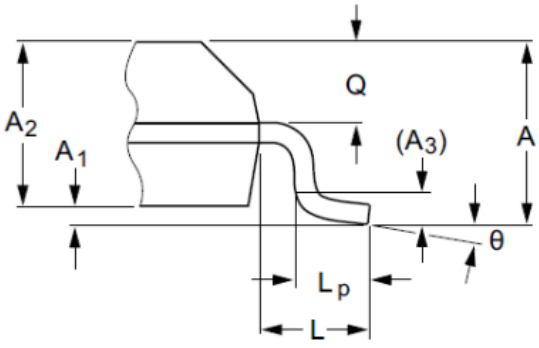


Figure 12

[*] Plastic or metal protrusions of 0.15 mm maximum per side are not included

Parameter	Min	Max	Unit
c	0.19	0.25	mm
E[*]	3.8	4.0	mm
H_E	5.8	6.2	mm
v	0.25	0.25	mm

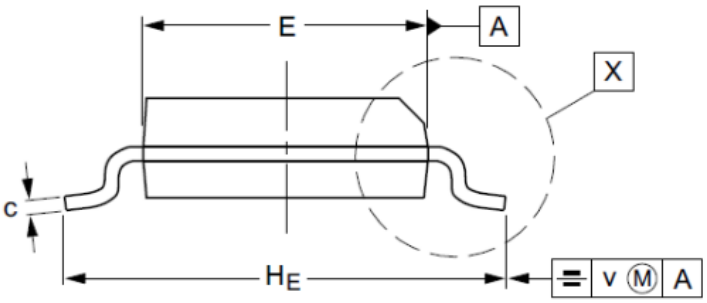


Figure 13

Parameter	Min	Max	Unit
b_p	0.36	0.49	mm
e	1.27	1.27	mm
w	0.25	0.25	mm
Z[*]	0.3	0.7	mm

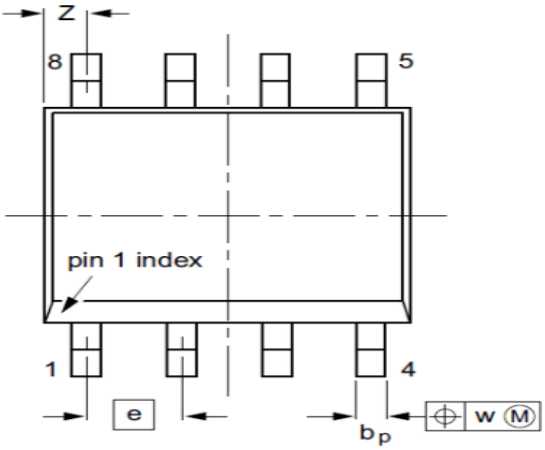


Figure 14

* Plastic or metal protrusions of 0.25 mm maximum per side are not included

16. Appendix: ISO 11898-2:2016 parameter

ISO 11898-2:2016		Datasheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA recessive output characteristics, bus biasing active/inactive			
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{O(rec)}$	Recessive output voltage
Single ended output voltage on CAN_L	V_{CAN_L}		
Differential output voltage	V_{Diff}	$V_{O(diff)}$	Differential output voltage
Optional HS-PMA transmit dominant timeout			
Transmit dominant timeout, long	t_{dom}	$t_{to(dom)TXD}$	TXD dominant time-out time
Transmit dominant timeout, short			
HS-PMA dominant output characteristics			
Single ended voltage on CAN_H	V_{CAN_H}	$V_{O(dom)}$	Dominant output voltage
Single ended voltage on CAN_L	V_{CAN_L}		
Differential voltage on normal bus load	V_{Diff}	$V_{O(diff)}$	Differential output voltage
Differential voltage on effective resistance during arbitration			
Optional: Differential voltage on extended bus load range			
HS-PMA driver symmetry			
Driver symmetry	V_{SYM}	V_{TXsym}	Transmitter voltage symmetry
Maximum HS-PMA driver output current			
Absolute current on CAN_H	I_{CAN_H}	$I_{O(sc)dom}$	Dominant short-circuit output current
Absolute current on CAN_L	I_{CAN_L}		
HS-PMA static receiver input characteristics, bus biasing active/inactive			
Recessive state differential input voltage range Dominant state differential input voltage range	V_{Diff}	$V_{th(RX)dif}$	Differential receiver threshold voltage
		$V_{rec(RX)}$	Receiver recessive voltage
		$V_{dom(RX)}$	Receiver dominant voltage
HS-PMA implementation loop delay requirement			
Loop delay	t_{Loop}	$t_{d(TXDH-RXDH)}$	Delay time from TXD HIGH to RXD HIGH
		$t_{d(TXDL-RXDL)}$	Delay time from TXD LOW to RXD LOW
HS-PMA receiver input resistance (matching)			
Differential internal resistance	R_{Diff}	$R_{i(dif)}$	Differential input resistance
Single ended internal resistance	R_{CAN_H} R_{CAN_L}	R_i	Input resistance
Matching of internal resistance	MR	ΔR_i	Input resistance deviation
Optional HS-PMA implementation data signal timing requirements for use with bit rates above 1 Mbit/s up to 2 Mbit/s and above 2 Mbit/s up to 5 Mbit/s			
Transmitted recessive bit width @ 2 Mbit/s / @ 5 Mbit/s, intended	$t_{Bit(Bus)}$	$t_{bit(bus)}$	Transmitted recessive bit width
Received recessive bit width @ 2 Mbit/s / @ 5 Mbit/s	$t_{Bit(RXD)}$	$t_{bit(RXD)}$	Bit time on pin RXD
Receiver timing symmetry @ 2 Mbit/s / @ 5 Mbit/s	Δt_{Rec}	Δt_{rec}	Receiver timing symmetry
HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered			
Leakage current on CAN_H, CAN_L	I_{CAN_H} I_{CAN_L}	I_L	Leakage current
HS-PMA maximum ratings of V_{CAN_H}, V_{CAN_L}, and V_{Diff}			
Maximum rating V_{Diff}	V_{Diff}	$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL

General maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	V_x	voltage on pin x
Optional: Extended maximum rating V_{CAN_H} and V_{CAN_L}			
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Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA bus biasing control timings			
CAN activity filter time, long	t_{Filter}	$t_{wake(bus-dom)}$[*] $t_{wake(bus-rec)}$	bus dominant wake-up time bus recessive wake-up time
CAN activity filter time, short			
Wake-up timeout, short	t_{Wake}	$t_{to(wake)bus}$	bus wake-up time-out time
Wake-up timeout, long			
Timeout for bus inactivity	$t_{Silence}$	$t_{to(silence)}$	bus silence time-out time
Bus Bias reaction time	t_{Bias}	$t_{d(busact-bias)}$	delay time from bus active to bias

* $t_{fltr(wake)bus}$ - bus wake-up filter time, in devices with basic wake-up functionality