# 1. Introduction

The local interconnect network (LIN) is a serial communication protocol, designed to support automotive networks in conjunction with a Controller Area Network (CAN) module. LIN is a single wire bidirectional bus typically used for low speed in-vehicle networks using data rates up to 20 kbps. As the lowest level of a hierarchical network, LIN enables cost effective communication with sensors and actuators when all the features of CAN communication are not required. They provide excellent EMC (Electromagnetic Compatibility) and Radiated Emission performance, ESD (Electrostatic Discharge) robustness, and safe behavior, in the event of a LIN bus short-to-ground, or a LIN bus leakage during low-power mode.

# 2. Features

- Operating supply range 6 V ≤ $V_{SUP}$ ≤ 26 V
- Wide input voltage range -40 V ≤ $V_{LIN}$ ≤ 40V
- Compliant to LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and ISO/DIS 17987–4.2
- Conforms to SAEJ2602 recommended practice for LIN
- Transmit data with baud rate up to 20 kbps
- Active bus wave shaping, offering excellent radiated emission performance
- Very high immunity against electro-magnetic interference
- Sustains up to 15.0 kV minimum ESD IEC61000-4-2 on the LIN Bus, 20 kV on the WAKE pin, and 25 kV on the VSUP pin
- Power up and down glitch free operation
- Control of external voltage regulator using INH pin
- Protection features:
  - Under voltage protection on VSUP
  - TXD dominant state time-out protection
  - Thermal shutdown
  - Unpowered node or ground disconnection fail-safe at system level
- Integrated input EMI filter
- Sleep mode: ultra-low current consumption allows wake up events from:
  - LIN bus
  - Wake up input (external switch)
  - Local wake up through EN
- Local and remote wake-up capability reported by RXD pin
- Fast baud rate selection (up to 100 kbps) reported by RXD pin
- Internal LIN slave termination resistor

# 3. Pinning Information

| PIN | | | | |
|---|---|---|---|---|
| NO. | Name | Function | Formal Name | Description |
| 1 | RXD | Output | Data Output | This pin is the receiver output of the LIN interface which reports the state of the bus voltage to the MCU interface |
| 2 | EN | Input | Enable Control | This pin controls the operation mode of the interface. |
| 3 | WAKE | Input | Wake Input | This pin is a high-voltage input used to wake-up the device from Sleep mode. |
| 4 | TXD | Input | Data Input | This pin is the transmitter input of the LIN interface which controls the state of the bus output. |
| 5 | GND | Ground | Ground | This pin is the device ground pin. |
| 6 | LIN | Input/Output | LIN Bus | This bidirectional pin represents the single-wire bus transmitter and receiver. |
| 7 | VSUP | Power | Power Supply | This pin is the device battery level power supply. |
| 8 | INH | Output | Inhibit Output | This pin can have two main functions: controlling an external switchable voltage regulator having an inhibit input, or driving an external bus resistor in the master node application. |

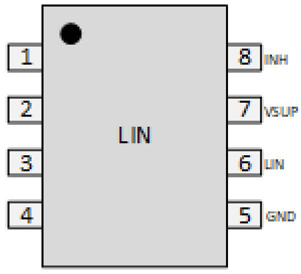



Figure 1: Pinning configuration

# 4. Quick Reference

| Symbol | Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{SUP}$ | Supply voltage | | -0.3 | 40 | V |
| $V_{LIN}$ | Bus voltage | | -40 | 40 | V |
| $V_{Wake}$ | Wake voltage | | -40 | $V_S$+0.3 | V |
| $V_{INH}$ | Inhibit voltage | | -0.3 | $V_S$+0.3 | V |
| $V_{TX,RX,EN}$ | Logic voltage[1] | | -0.3 | 5.5 | V |
| $I_{CC}$ | Supply current in sleep mode | $V_{SUP} \leq 13.5$ V, Recessive State<br>13.5 V < $V_{SUP}$ < 27 V<br>$V_{SUP} \leq 13.5$ V, Shorted to GND | -<br>-<br>- | 197<br>208<br>200 | µA<br>µA<br>µA |
| | Supply current in normal or slow or fast mode | Bus Recessive, Excluding INH Output Current<br>Bus Dominant, Excluding INH Output Current | -<br>- | 0.62<br>1.3 | mA<br>mA |
| $T_j$ | Junction temperature | | -40 | 150 | °C |

[1] At $V_S$ > 5.5 v

# 5. Ordering Information

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| | SO8 | plastic small outline package; 8 leads; body width 3.9 mm | |

# 6. Block Diagram

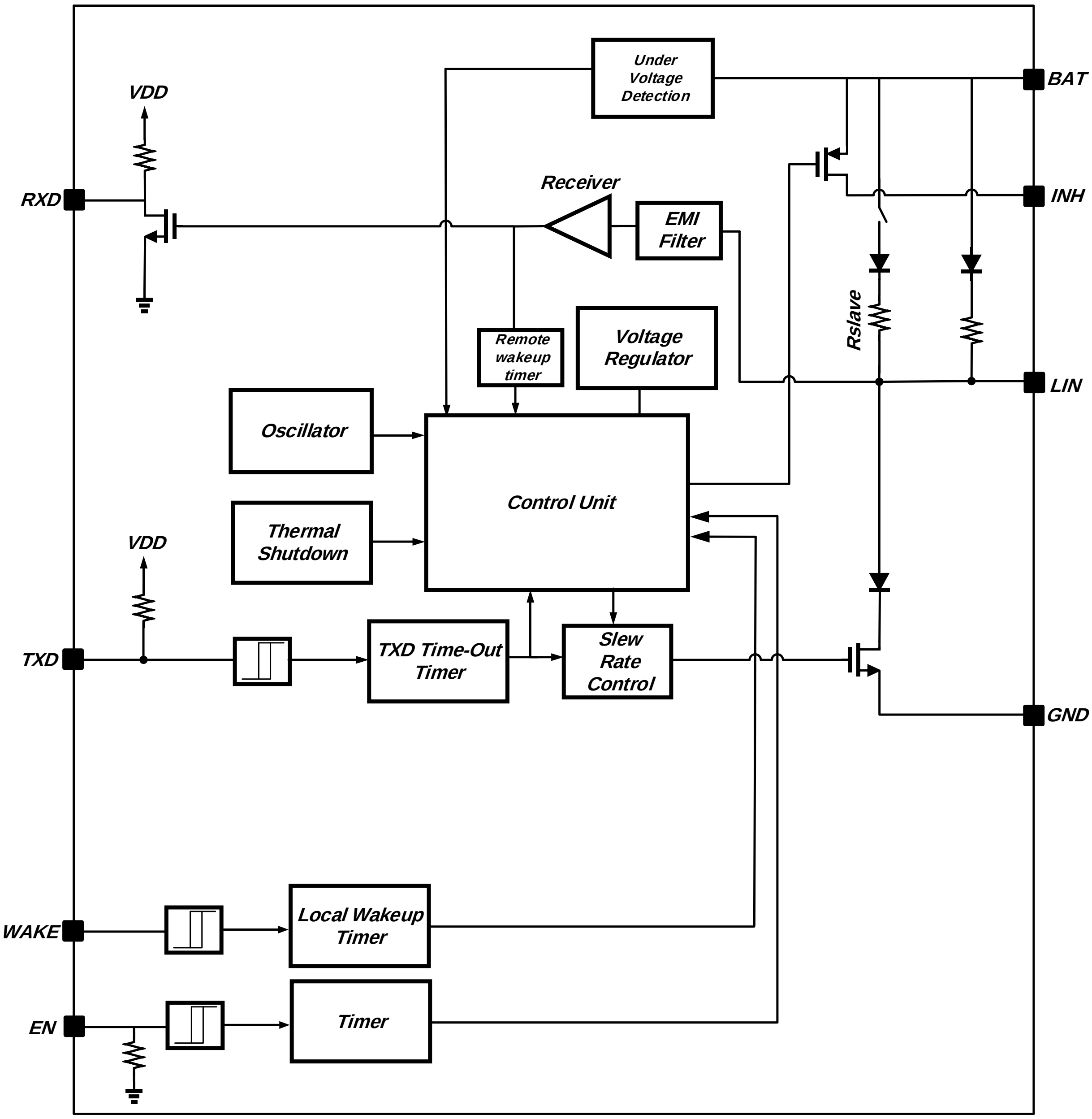



Figure 2: Block diagram

# 7. Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Ratings | Symbol | Value | Unit |
|---|---|---|---|
| **Electrical Ratings** | | | |
| Power Supply Voltage | | | V |
| Normal Operation (DC) | $V_{SUP(SS)}$ | -0.3 to 27 | |
| Transient input voltage with external component (according to ISO7637-2 & ISO7637-3 & "Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications") (See Figure 13) | | | |
| Pulse 1 (test up to the limit for damage - Class A[1]) | $V_{SUP(S1)}$ | -100 | |
| Pulse 2a (test up to the limit for damage - Class A[1]) | $V_{SUP(S2A)}$ | +75 | |
| Pulse 3a (test up to the limit for damage - Class A[1]) | $V_{SUP(S3A)}$ | -150 | |
| Pulse 3b (test up to the limit for damage - Class A[1]) | $V_{SUP(S3B)}$ | +100 | |
| Pulse 5b (Class A)[1] | $V_{SUP(S5B)}$ | -0.3 to 40 | |
| WAKE | | | |
| Normal Operation within series 2*18 kΩ resistor (DC) | $V_{WAKE(SS)}$ | -27 to 40 | |
| Transient input voltage with external component (according to ISO7637-2 & ISO7637-3 & "Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications") (See Figure 14) | | | |
| Pulse 1 (test up to the limit for damage - Class D[2]) | $V_{WAKE(S1)}$ | -100 | |
| Pulse 2a (test up to the limit for damage - Class D[2]) | $V_{WAKE(S2A)}$ | +75 | |
| Pulse 3a (test up to the limit for damage - Class D[2]) | $V_{WAKE(S3A)}$ | -150 | |
| Pulse 3b (test up to the limit for damage - Class D[2]) | $V_{WAKE(S3B)}$ | +100 | |
| Logic voltage (RXD, TXD, EN Pins) | $V_{LOG}$ | - 0.3 to 5.5 | |
| LIN Bus Voltage | | | |
| Normal Operation (DC) | $V_{BUS(SS)}$ | -27 to 40 | |
| Transient (coupled through 1.0 nF capacitor, according to ISO7637-2 & ISO7637-3 & "Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications") (See Figure 15) | | | |
| Pulse 1 (test up to the limit for damage - Class D[2]) | $V_{BUS(S1)}$ | -100 | |
| Pulse 2a (test up to the limit for damage - Class D[2]) | $V_{BUS(S2A)}$ | +75 | |
| Pulse 3a (test up to the limit for damage - Class D[2]) | $V_{BUS(S3A)}$ | -150 | |
| Pulse 3b (test up to the limit for damage - Class D[2]) | $V_{BUS(S3B)}$ | +100 | |
| INH voltage /current | | | |
| DC Voltage | $V_{INH}$ | -0.3 to $V_{SUP}$ +0.3 | |
| Transient (coupled through 1.0 nF capacitor, according to ISO7637-2 & ISO7637-3 & "Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications") (See Figure 16) | | | |
| Pulse 1 (test up to the limit for damage - Class D[2]) | $V_{INH(S1)}$ | -100 | |
| Pulse 2a (test up to the limit for damage - Class D[2]) | $V_{INH(S2A)}$ | +75 | |
| Pulse 3a (test up to the limit for damage - Class D[2]) | $V_{INH(S3A)}$ | -150 | |
| Pulse 3b (test up to the limit for damage - Class D[2]) | $V_{INH(S3B)}$ | +100 | |

[1] Class A: All functions of a device/system perform as designed during and after exposure to disturbance

[2] Class D: At least one function of the transceiver stops working properly during the test, and will return to proper operation automatically when the exposure to the disturbance has ended. No physical damage of the IC occurs.

| Ratings | Symbol | Value | Unit |
|---|---|---|---|
| **Electrical Ratings** | | | |
| ESD Capability - AECQ100<br>Human Body Model - JESD22/A114 ($C_{ZAP}$ = 100 pF, $R_{ZAP}$ = 1500 Ω) | | | V |
| LIN pin versus GND | $V_{ESD1-1}$ | ±10.0 k | |
| Wake pin versus GND | $V_{ESD1-2}$ | ±8.0 k | |
| All other pins | $V_{ESD1-4}$ | ±4.0 k | |
| According to "Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications" ($C_{ZAP}$ = 150 pF, $R_{ZAP}$ = 330 Ω)<br>Contact Discharge, Unpowered | | | |
| LIN pin without capacitor | $V_{ESD4-1}$ | ±15 k | |
| LIN pin with 220 pF capacitor | $V_{ESD4-2}$ | ±15 k | |
| $V_{SUP}$ (10 µF to ground) | $V_{ESD4-3}$ | ±25 k | |
| WAKE (2*18 kΩ serial resistor | $V_{ESD4-4}$ | ±20 k | |
| INH pin | $V_{ESD4-5}$ | ±2.0 k | |
| LIN pin with 220 pF capacitor and indirect ESD coupling (according to ISO10605 - Annex F) | $V_{ESD4-6}$ | >±15 k | |
| According to ISO10605<br>(2.0 kΩ / 150 pF) - Unpowered - Contact discharge | | | |
| LIN pin without capacitor | $V_{ESD5-1}$ | ±20 k | |
| LIN pin with 220 pF capacitor | $V_{ESD5-2}$ | ±25 k | |
| $V_{SUP}$ (10 µF to ground) | $V_{ESD5-3}$ | ±25 k | |
| WAKE (2*18 kΩ serial resistor) | $V_{ESD5-4}$ | ±25 k | |
| (2.0 kΩ / 330 pF) - Powered - Contact discharge | | | |
| LIN pin without capacitor | $V_{ESD6-1}$ | ±8 k | |
| LIN pin with 220 pF capacitor | $V_{ESD6-2}$ | ±10 k | |
| $V_{SUP}$ (10 µF to ground) | $V_{ESD6-3}$ | ±12 k | |
| WAKE (2*18 kΩ serial resistor) | $V_{ESD6-4}$ | ±15 k | |
| **Thermal Ratings** | | | |
| Operating temperature | | | °C |
| Ambient | $T_A$ | -40 to 125 | |
| Junction | $T_J$ | -40 to 125 | |
| Storage temperature | $T_{STG}$ | -40 to 150 | °C |
| Thermal resistance, junction to ambient | $R_{\theta JA}$ | 150 | °C/W |
| Peak package reflow temperature during solder mounting[1] | $T_{SOLDER}$ | 240 | °C |
| Thermal shutdown temperature | $T_{SHUT}$ | 150 to 200 | °C |
| Thermal shutdown hysteresis temperature | $T_{HYST}$ | 20 | °C |

[1] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

# 8. Static Electrical Characteristics

Characteristics under conditions 7.0 V ≤ $V_{SUP}$ ≤ 18 V, -40°C ≤ $T_A$ ≤ 125°C, GND = 0 V, unless otherwise noted. Typical values reflect the approximate parameter means at $T_A$ = 25°C under nominal conditions, unless otherwise noted.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **$V_{SUP}$ Pin (Device Power Supply)** | | | | | | |
| $V_{SUP}$ | Nominal Operating Voltage | | -0.3 | 13.5 | 18.0 | V |
| $V_{SUPOP}$ | Functional Operating Voltage[1] | | 7 | - | 30 | V |
| $V_{SUPLD}$ | Load Dump | | - | - | 40 | V |
| $V_{POR}$ | Power-On Reset (POR) Threshold | $V_{SUP}$ Ramp Down and INH goes High to Low | 3.7 | - | 5.4 | V |
| $V_{PORHYST}$ | Power-On Reset (POR) Hysteresis | | - | 350 | - | mV |
| $V_{UVL}$, $V_{UVH}$ | $V_{SUP}$ Under-Voltage Threshold (positive and negative) | Transmission disabled and LIN bus goes in recessive state | 4.7 | - | 6 | V |
| $V_{UVHYST}$ | $V_{SUP}$ Under-Voltage Hysteresis ($V_{UVL}$ - $V_{UVH}$) | | - | 300 | - | mV |
| $I_{CC}$ | Supply Current in Sleep Mode | $V_{SUP}$ ≤ 13.5 V, Recessive State | - | 45 | 197 | µA |
| | | 13.5 V < $V_{SUP}$ < 27 V | - | 55 | 208 | µA |
| | | $V_{SUP}$ ≤ 13.5 V, Shorted to GND | - | 50 | 200 | µA |
| | Supply Current in Normal or Slow or Fast Mode | Bus Recessive, Excluding INH Output Current | - | 0.4 | 0.62 | mA |
| | | Bus Dominant, Excluding INH Output Current | - | 1 | 1.3 | mA |
| **RXD Output Pin (Logic)** | | | | | | |
| $V_{OL}$ | Low Level Output Voltage | $I_{IN}$ ≤ 1.5 mA | 0.2 | - | 0.5 | V |
| $V_{OH}$ | High Level Output Voltage | $V_{EN}$ = 5.0 V, $I_{OUT}$ ≤ 250 µA | 4.25 | - | 5.34 | V |
| **TXD Input Pin (Logic)** | | | | | | |
| $V_{IL}$ | Low Level Input Voltage | | - | - | 2.0 | V |
| $V_{IH}$ | High Level Input Voltage | | 4.0 | - | - | V |
| $V_{INHYST}$ | Input Threshold Voltage Hysteresis | | 0.4 | 1 | 2 | V |
| $I_{PU}$ | Pull-up Current Source | $V_{EN}$ = 5.0 V, 1.0 V < $V_{TXD}$ < 3.5 V | -80 | -60 | -40 | µA |
| **EN Input Pin (Logic)** | | | | | | |
| $V_{IL}$ | Low Level Input Voltage | | - | - | 2.0 | V |
| $V_{IH}$ | High Level Input Voltage | | 4.0 | - | - | V |
| $V_{INHYST}$ | Input Voltage Threshold Hysteresis | | 0.4 | 1.3 | 2 | V |
| $R_{PD}$ | Pull-down Resistor | | 80 | 85 | 300 | kΩ |
| **LIN Physical Layer- Transceiver LIN[2]** | | | | | | |
| $V_{BAT}$ | Operating Voltage Range[3] | | 7.0 | - | 18 | V |
| $V_{SUP}$ | Supply Voltage Range | | 7.0 | - | 18 | V |
| $V_{SUP\_NON\_OP}$ | Voltage Range (within which the device is not destroyed) | | -0.3 | - | 40 | V |

[1] For the functional operating voltage, the device is functional and all features are operating. The electrical parameters are noted under conditions 7.0 V ≤ $V_{SUP}$ ≤ 18 V, -40°C ≤ $T_A$ ≤ 125°C, GND = 0 V.

[2] Parameters guaranteed for 7.0 V ≤ $V_{SUP}$ ≤ 18 V

[3] Voltage range at the battery level, including the reverse battery diode.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{BUS\_LIM}$ | Current Limitation for Driver Dominant State | Driver on, $V_{BUS}$ = 18 V | 60 | 70 | 80 | mA |
| $I_{BUS\_PAS\_DOM}$ | Input Leakage Current at the Receiver | Driver off; $V_{BUS}$ = 0 V; $V_{BAT}$ = 12 V | -0.368 | - | - | mA |
| $I_{BUS\_PAS\_REC}$ | Leakage Output Current to GND | Driver Off; 8.0 V < $V_{BAT}$ < 18 V; 8.0 V < $V_{BUS}$ < 18 V; $V_{BUS} \geq V_{BAT}$; $V_{BUS} \geq V_{SUP}$ | - | - | 20 | µA |
| $I_{BUS\_NO\_GND}$ | | Control Unit Disconnected from Ground[1] $GND_{DEVICE}$ = $V_{SUP}$; $V_{BAT}$ = 12 V; 0 < $V_{BUS}$ < 18 V | -1.0 | - | 1.0 | mA |
| $I_{BUS\_NO\_BAT}$ | | $V_{BAT}$ Disconnected; $V_{SUP\_DEVICE}$ = GND; 0 V < $V_{BUS}$ < 18 V[2] | - | - | 100 | µA |
| $V_{BUSDOM}$ | Receiver Dominant State[3] | | - | - | 0.4 | $V_{SUP}$ |
| $V_{BUSREC}$ | Receiver Recessive State[4] | | 0.6 | - | - | $V_{SUP}$ |
| $V_{BUS\_CNT}$ | Receiver Threshold Center ($V_{TH\_DOM}$ + $V_{TH\_REC}$)/2 | | 0.475 | 0.5 | 0.525 | $V_{SUP}$ |
| $V_{HYS}$ | Receiver Threshold Hysteresis ($V_{TH\_DOM}$ - $V_{TH\_REC}$) | | - | - | 0.175 | $V_{SUP}$ |
| $R_{SLAVE}$ | LIN Pull-up Resistor to $V_{SUP}$ | | 20 | 30 | 60 | kΩ |
| $C_{LIN}$ | LIN Internal Capacitor[5] | | - | - | 250 | pF |
| **INH Output Pin** | | | | | | |
| $INH_{ON}$ | Driver On Resistance (Normal Mode) | $I_{INH}$ = 50 mA | - | 20 | 50 | Ω |
| $I_{INH\_LOAD}$ | Current load capability | From 7.0 V < $V_{SUP}$ < 18 V | - | - | 30 | mA |
| $I_{LEAK}$ | Leakage Current (Sleep Mode) | 0 < $V_{INH}$ < $V_{SUP}$ | -5.0 | - | 5.0 | µA |
| **WAKE Input Pin** | | | | | | |
| $V_{WUHL1}$ | High to Low Detection Threshold | 5.5 V < $V_{SUP}$ < 7 V | 2.0 | - | 3.9 | V |
| $V_{WULH1}$ | Low to High Detection Threshold | 5.5 V < $V_{SUP}$ < 7 V | 2.4 | - | 4.3 | V |
| $V_{WUHYS1}$ | Hysteresis | 5.5 V < $V_{SUP}$ < 7 V | 0.2 | - | 0.8 | V |
| $V_{WUHL2}$ | High to Low Detection Threshold | 7 V ≤ $V_{SUP}$ < 26 V | 2.4 | - | 3.9 | V |
| $V_{WULH2}$ | Low to High Detection Threshold | 7 V ≤ $V_{SUP}$ < 26 V | 2.9 | - | 4.3 | V |
| $V_{WUHYS2}$ | Hysteresis | 7 V ≤ $V_{SUP}$ < 26 V | 0.2 | - | 0.8 | V |
| $I_{WU}$ | Wake-up Input Current | $V_{WAKE}$ < 27 V | - | - | 3.0 | µA |

# 9. Dynamic Electrical Characteristics

Characteristics under conditions 7.0 V ≤ $V_{SUP}$ ≤ 18 V, -40°C ≤ $T_A$ ≤ 125°C, GND = 0 V, unless otherwise noted. Typical values reflect the approximate parameter means at $T_A$ = 25°C under nominal conditions, unless otherwise noted.

[1] Loss of local ground must not affect communication in the residual network.

[2] Node has to sustain the current that can flow under this condition. The bus must remain operational under this condition.

[3] LIN threshold for a dominant state.

[4] LIN threshold for a recessive state.

[5] This parameter is guaranteed by process monitoring but not production tested.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **LIN Physical Layer**<br>**Driver Characteristics For Normal Slew Rate - 20.0 KBIT/SEC[1,2]** | | | | | | |
| D1 | Duty Cycle 1:<br>$TH_{REC(MAX)} = 0.744 * V_{SUP}$<br>$TH_{DOM(MAX)} = 0.581 * V_{SUP}$<br>$D1 = t_{BUS\_REC(MIN)}/(2 \times t_{BIT})$, $t_{BIT} = 50$ µs, $7.0\ V \leq V_{SUP} \leq 18\ V$ | | 0.396 | - | - | % |
| D2 | Duty Cycle 2:<br>$TH_{REC(MIN)} = 0.422 * V_{SUP}$<br>$TH_{DOM(MIN)} = 0.284 * V_{SUP}$<br>$D2 = t_{BUS\_REC(MAX)}/(2 \times t_{BIT})$, $t_{BIT} = 50$ µs, $7.6\ V \leq V_{SUP} \leq 18\ V$ | | - | - | 0.581 | % |
| **LIN Physical Layer**<br>**Driver Characteristics For Fast Slew Rate** | | | | | | |
| $BR_{FAST}$ | Fast Bit Rate (Programming Mode) | | - | - | 100 | kbit/ sec |
| **LIN Physical Layer**<br>**Transmitter Characteristics For Normal Slew Rate - 20.0 KBIT/SEC[3]** | | | | | | |
| $t_{TRAN\_SYM}$ | Symmetry of Transmitter delay[4]<br>$t_{TRAN\_SYM} = MAX(t_{TRAN\_SYM60\%}, t_{TRAN\_SYM40\%})$<br>$t_{TRAN\_SYM60\%} = \lvert t_{TRAN\_PDF60\%} - t_{TRAN\_PDR60\%} \rvert$<br>$t_{TRAN\_SYM40\%} = \lvert t_{TRAN\_PDF40\%} - t_{TRAN\_PDR40\%} \rvert$ | | -7.25 | - | 7.25 | µs |
| **LIN physical Layer**<br>**Receiver Characteristics[5]** | | | | | | |
| $t_{REC\_PD}$ | Propagation Delay of Receiver, $t_{REC\_PD} = MAX(t_{REC\_PDR}, t_{REC\_PDF})$[6] | | - | - | 6.0 | µs |
| $t_{REC\_SYM}$ | Symmetry of Receiver Propagation Delay, $t_{REC\_PDF} - t_{REC\_PDR}$[6] | | -0.5 | - | 0.5 | µs |
| **Wake-Up Timings** | | | | | | |
| $t_{WUF}$ | Bus Wake-up Deglitcher | Sleep Mode | 40 | 70 | 100 | µs |
| $t_{LWUE}$ | EN Wake-up Deglitcher[7] | EN High to INH Low to High | - | 9 | 15 | µs |
| $t_{WF}$ | Wake-up Deglitcher | Wake state change to INH Low to High | 10 | 48 | 70 | µs |
| **First Dominant Bit Validation** | | | | | | |
| $t_{FIRST\_DOM}$ | First dominate bit validation delay | Normal Mode | - | 45 | 80 | µs |
| **Sleep Mode** | | | | | | |
| $t_{SD}$ | Sleep Mode Delay Time | After EN High to Low to INH High to Low with 100 µA load on INH | 50 | 60 | 91 | µs |
| **TXD Timing** | | | | | | |
| $t_{TXDDOM}$ | TXD Permanent Dominant State Delay[8] | | 3.75 | 4.0 | 6.25 | ms |

[1] Bus load $R_{BUS}$ and $C_{BUS}$ 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 3.

[2] See Figure 4.

[3] $V_{SUP}$ from 7.0 to 18 V, bus load $R_{BUS}$ and $C_{BUS}$ 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 3.

[4] See Figure 5.

[5] $V_{SUP}$ from 7.0 to 18 V, bus load $R_{BUS}$ and $C_{BUS}$ 1.0 nF / 1.0 k Ω, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 3.

[6] See Figure 6.

[7] See Figure 7.

[8] The LIN is in recessive state and the receiver is still active.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Fast Baud Rate Timing** | | | | | | |
| $t_1$ | EN Low Pulse Duration to Enter in Fast Baud Rate using Toggle Function[1] | EN High to Low and Low to High | - | - | 45 | µs |
| $t_2$ | TXD Low Pulse Duration to Enter in Fast Baud Rate using Toggle Function[1] | | 12.5 | - | - | µs |
| $t_3$ | Delay Between EN Falling Edge and TXD Falling Edge to Enter in Fast Baud Rate Using Toggle Function[1] | | 12.5 | - | - | µs |
| $t_4$ | Delay Between TXD Rising Edge and EN Rising Edge to Enter in Fast Baud Rate Using Toggle Function[1] | | 12.5 | - | - | µs |
| $t_5$ | RXD Low Level duration after EN rising edge to validate the Fast Baud Rate entrance[1] | | 1.875 | | 6.25 | µs |

## 9.1 Timing Diagrams

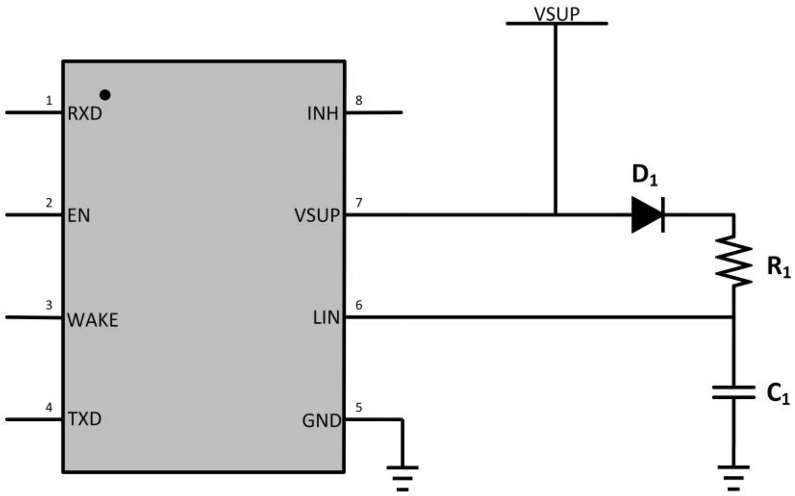



Figure 3: Test circuit for timing measurements

[1] See Figure 8 and 9.

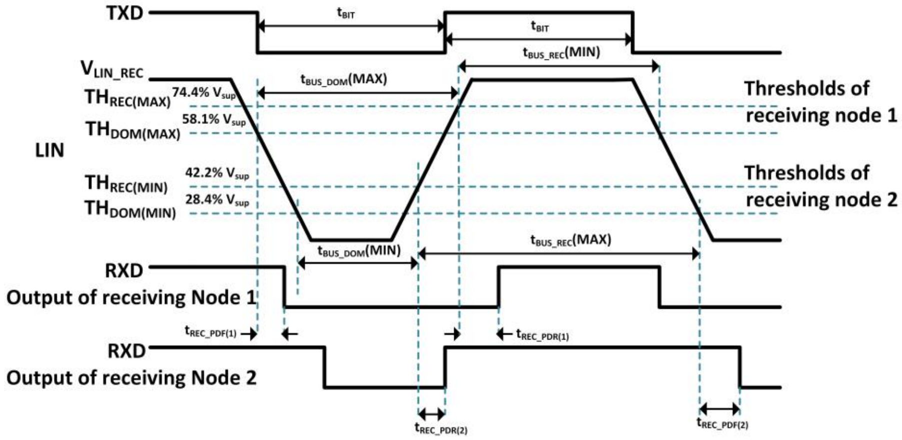



Figure 4: LIN timing measurements for normal baud rate

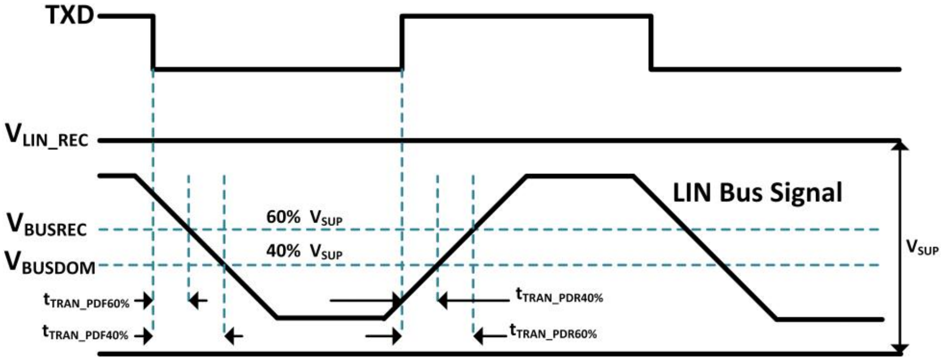



Figure 5: LIN transmitter timing

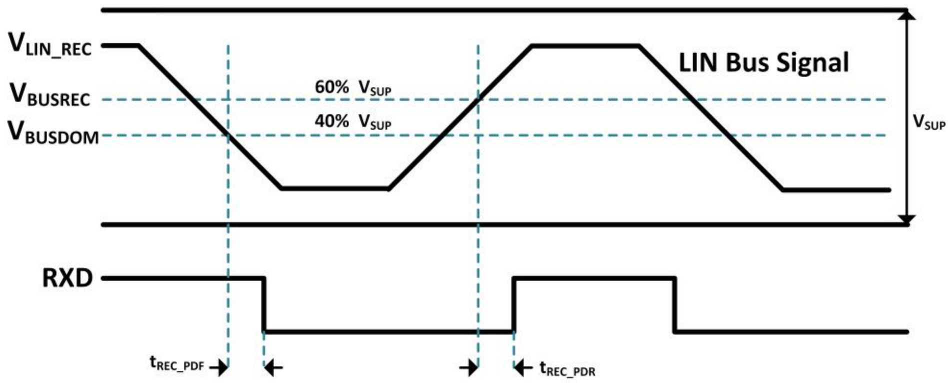



Figure 6: LIN receiver timing

## 9.2 Functional Diagrams

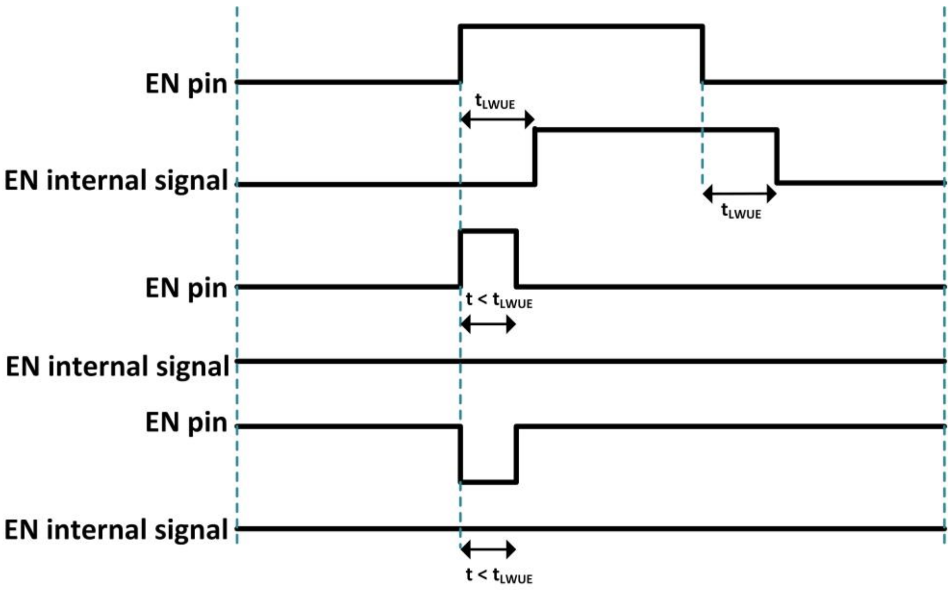



Figure 7: EN pin deglitcher

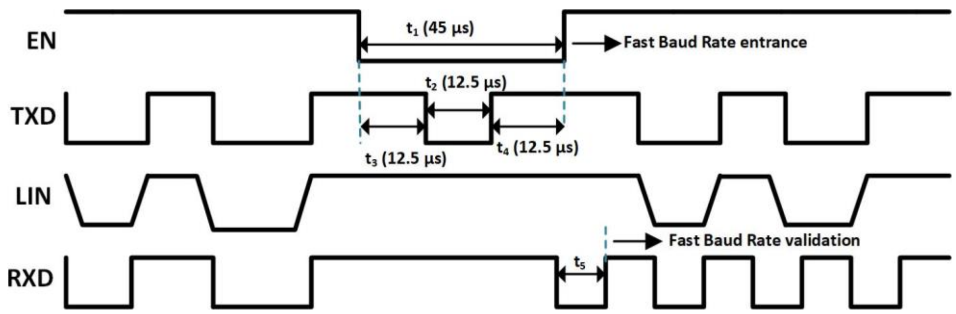



Figure 8: Fast baud rate selection (Toggle Function)

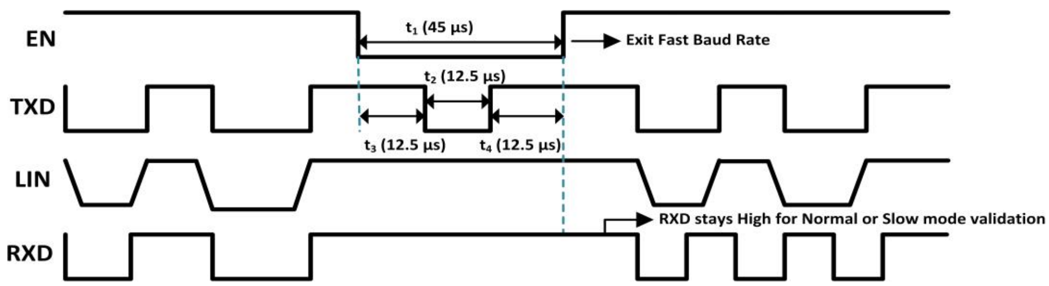



Figure 9: Fast baud rate mode exit (back to normal or slow slew rate)

# 10. Functional Pin Description

## 10.1 Data Output Pin (RXD)

RXD output pin is the MCU interface, which reports the state of the LIN bus voltage. In Normal or Slow baud rate, LIN high (recessive) is reported by a high voltage on RXD; LIN low (dominant) is reported by a low voltage on RXD. The RXD output structure is a tristate output buffer (See Figure 10). The RXD output pin is the receiver output of the LIN interface. The low level is fixed. The high level is dependent on EN voltage. In Sleep mode, RXD is high-impedance. When a wake-up event is recognized from the WAKE pin or from the LIN bus pin, RXD is pulled LOW to report the wake-up event. An external pull-up resistor may be needed.

## 10.2 Enable Input Pin (EN)

EN input pin controls the operation mode of the interface. If EN = 1, the interface is in Normal mode, TXD to LIN after $t_{FIRST\_DOM}$ delay and LIN to RXD paths are both active. RXD $V_{OH}$ level follows EN pin high level. The device enters the Sleep mode by setting EN LOW for a delay higher than $t_{SD}$ (70 µs typ. value) and if the WAKE pin state doesn't change during this delay. A combination of the logic levels on the EN and TXD pins allows the device to enter into the Fast Baud Rate mode of operation (see Figure 8).

## 10.3 Wake Input Pin (WAKE)

The WAKE pin is a high voltage input used to wake-up the device from the Sleep mode. WAKE is usually connected to an external switch in the application. The WAKE pin has a special design structure and allows wake-up from both high to low or low to high transitions. When entering into sleep mode, the device monitors the state of the WAKE pin and stores it as a reference state. The opposite state of this reference state will be the wake-up event used by the device to enter again structure exhibits a high-impedance, with extremely low input current when voltage at this pin is below 27 V. Two serial resistors should be inserted in order to limit the input current mainly during transient pulses and ESD. The total recommended resistor value is 33 kΩ. An external 10 to 100 nF capacitor is advised for better EMC and ESD performances.

## 10.4 Data Input Pin (TXD)

The TXD input pin is the MCU interface to control the state of the LIN output. When TXD is low (dominant), LIN output is low; when TXD is high (recessive), the LIN output transistor is turned off. This pin has an internal pull-up current source to force the recessive state if the input pin is left floating. If the pin stays low (dominant sate) more than 5.0 ms (typical value), the LIN transmitter goes automatically into recessive state.

## 10.5 Ground Pin (GND)

In case of a ground disconnection at the module level, device does not have significant current consumption on the LIN bus pin when in the recessive state.

## 10.6 LIN Bus Pin (LIN)

The LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems. The LIN interface is only active during normal mode (See Figure 11). LIN bus short-to-ground, or a LIN bus leakage during low power mode. The INH output can be used to control an external voltage regulator, or to drive a LIN bus pull-up resistor.

### 10.6.1 Transmitter Characteristics

The LIN driver is a low side MOSFET with internal overcurrent thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated so no external pull-up components are required for the application in a slave node. An additional pull-up resistor of 1.0 kΩ must be added when the device is used in the master node. The LIN pin exhibits no reverse current from the LIN bus line to

$V_{SUP}$, even in the event of a GND shift or $V_{SUP}$ disconnection. As soon as the device enters in Normal mode, the LIN transmitter will be able to send the first dominant bit only after the $t_{FIRST\_DOM}$ delay. $t_{FIRST\_DOM}$ delay has no impact on the receiver. The receiver will be enabled as soon as the device enters in Normal mode.

### 10.6.2 Receiver Characteristics

The receiver thresholds are ratio-metric with the device supply pin. If the $V_{SUP}$ voltage goes below the $V_{SUP}$ under-voltage threshold ($V_{UVL}$, $V_{UVH}$), the bus enters into a recessive state even if communication is sent to TXD. In case of LIN thermal shutdown, the transceiver and receiver are in recessive and INH turned off. When the temperature is below the $T_{LINSD}$, INH and LIN will be automatically enabled. The fast Baud Rate selection is reported by the RXD pin. Fast Baud Rate is activated by the toggle function (See Figure 8). At the end of the toggle function, just after EN rising edge, RXD pin is kept low for $t_5$ to flag the fast Baud Rate entry (See Figure 8). To exit the fast Baud Rate and return in normal or slow Baud Rate, a toggle function is needed. At the end of the toggle function, the RXD pin stays high to signal Fast Baud Rate exit (See Figure 9). The device enters into Fast Baud Rate at room and hot temperature.

## 10.7 Power Supply Pin ($V_{SUP}$)

The $V_{SUP}$ supply pin is the power supply pin. In an application, the pin is connected to a battery through a serial diode, for reverse battery protection. The DC operating voltage is from 7.0 to 18 V. This pin can sustain a standard automotive load dump condition up to 40 V. To avoid a false bus message, an under-voltage on $V_{SUP}$ disables the transmission path (from TXD to LIN) when $V_{SUP}$ falls below 6.7 V. Supply current in Sleep mode is typically 6.0 µA.

## 10.8 Inhibit Output Pin(INH)

The INH output pin is connected to an internal high side power MOSFET. The pin has two possible main functions. It can be used to control an external switchable voltage regulator having an inhibit input. It can also be used to drive the LIN bus external resistor in the master node application, thanks to its high drive capability. In Sleep mode, INH is turned off. If a voltage regulator inhibit input is connected to INH, the regulator will be disabled. If the master node pull-up resistor is connected to INH, the pull-up resistor will be unpowered and left floating. In case of a INH thermal shutdown, the high side is turned off and the LIN transmitter and receiver are in recessive state. An external 10 to 100 pF capacitor on INH pin is advised in order to improve EMC performances.

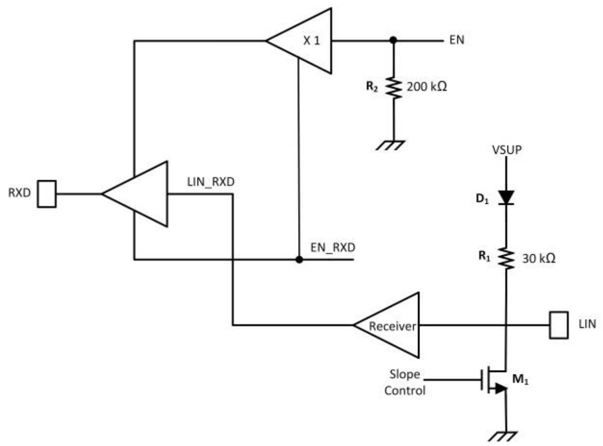



**Figure 10: RXD interface**

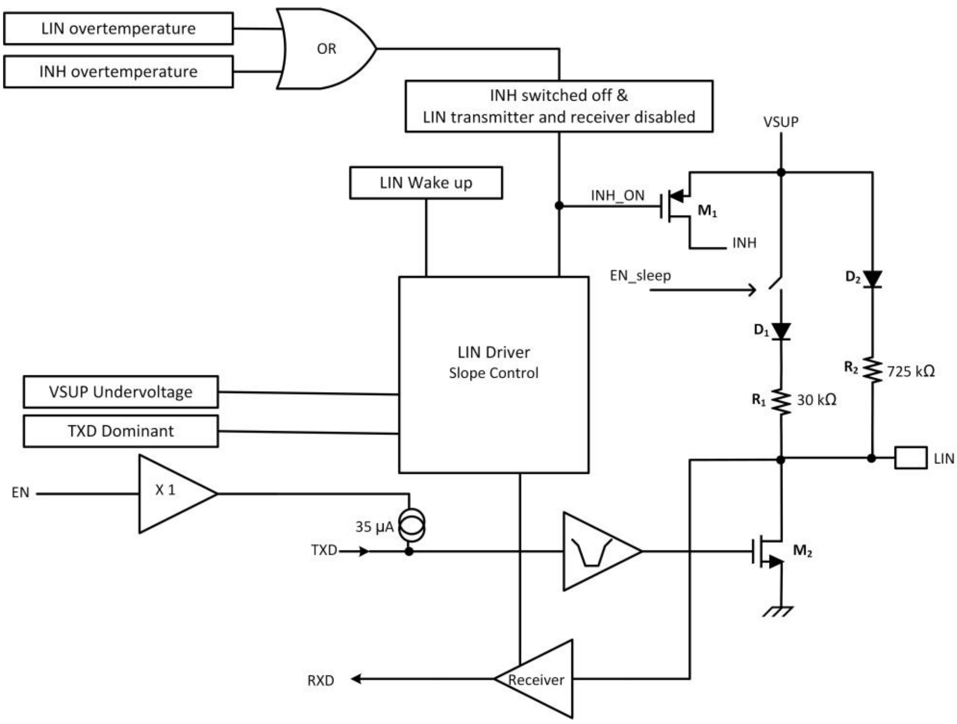



Figure 11: LIN Interface

# 11. Operational Modes

As described below, the device has two operational modes, Normal and Sleep. In addition, there are two transitional modes: Awake mode and Preparation to Sleep mode. The Awake mode allows the device to go into Normal mode. The Preparation to Sleep mode allows the device to go into Sleep mode.

## 11.1 Normal or Slow Baud Rate

In the Normal mode, the LIN bus can transmit and receive information. At normal Baud Rate (20 kbps) device has a slew rate and timing compatible with Normal Baud Rate. From Normal mode, the device can enter into Fast Baud Rate (Toggle function).

## 11.2 Fast Baud Rate

In Fast Baud Rate, the slew rate is around 10 times faster than the Normal Baud Rate. This allows very fast data transmission (more than 100 kbps). For instance, for electronic control unit (ECU) tests and microcontroller program download. The bus pull-up resistor might be adjusted to ensure a correct RC time constant in line with the high baud rate used. Fast Baud Rate is entered via a special sequence (called toggle function) as follows:

1- EN pin set LOW while TXD is High
2- TXD stays High for 12.5 µs
3- TXD set Low for 12.5 µs
4- TXD pulled HIGH for 12.5 µs
5- EN pin set Low to High while TXD still Highline

The device enters into the Fast Baud Rate if the delay between Step 1 to Step 5 is 45 µs maximum. The same toggle function is used to bring the device back into Normal Baud Rate. Fast Baud Rate selection is reported to the MCU by RXD pin. When the device returns in Normal Baud Rate with the same toggle function, the RXD pin stays high.

## 11.3 Preparation to Sleep Mode

To enter the Preparation to Sleep mode, EN must be low for a delay higher than $t_{LWUE}$. If the WAKE pin state doesn't change during $t_{SD}$ and $t_{LWUE}$ then the device goes into Sleep mode. If the WAKE pin state changes during $t_{SD}$ and if $t_{WF}$ is reached after end of $t_{SD}$ then the device goes into Sleep mode after the end of $t_{SD}$ timing. If the WAKE pin state changes during $t_{SD}$ and $t_{WF}$ delay has been reached before the end of $t_{SD}$ then the device goes into Awake mode. If the WAKE pin state changes before $t_{SD}$ and the delay $t_{WF}$ ends during $t_{SD}$ then the device goes into Awake mode. If EN goes high for a delay higher than $t_{LWUE}$, the device returns to Normal mode.

## 11.4 Sleep Mode

To enter into Sleep mode, EN must be low for a delay longer than $t_{SD}$ and the Wake pin must stay in the same state (High or Low) during this delay. In Sleep mode, the transmission path is disabled and the device is in Low Power mode. Supply current from $V_{SUP}$ is very low (6.0 µA typical value). Wake-up can occur from LIN bus activity, from the EN pin and from the WAKE input pin. If during the preparation to Sleep mode delay ($t_{SD}$), the LIN bus goes low due to LIN network communication, the device still enters into the Sleep mode. The device can be awakened by a recessive to dominant start, followed by a dominant to recessive state after t > $t_{WUF}$. After a Wake-up event, the device enters into Awake mode. In the Sleep mode, the internal 725 kΩ pull-up resistor is connected and the 30 kΩ is disconnected.

## 11.5 Device Power-Up (Awake Transitional Mode)

At power-up ($V_{SUP}$ rises from zero), when $V_{SUP}$ is above the Power On Reset voltage, the device automatically switches after a 160 µs delay time to the Awake transitional mode. It switches the INH pin to a High state and RXD to a Low state.

### 11.5.1Device Wake-Up Events

The device can be awakened from Sleep mode by three wake-up events:

- Remote wake-up via LIN bus activity: The device is awakened by a LIN dominant pulse longer than $t_{WUF}$. Dominant pulse means: a recessive to dominant transition, wait for t > $t_{WUF}$, then a dominant to recessive. Once the wake-up is detected (during the dominant to recessive transition), the device enters into Awake mode, with INH High and RXD pulled Low. Once in the Awake mode, the EN pin has to be set to 5.0 V to enter into Normal mode. Once in Normal mode, the device has to wait $t_{FIRST\_DOM}$ delay before transmitting the first dominant bit.

- Via the EN pin: The device can be waked-up by a Low to High transition of the EN pin. When EN is switched from LOW to HIGH and stays HIGH for a delay higher than $t_{LWUE}$, the device is awakened and enters into Normal mode. Once in Normal mode, the device has to wait $t_{FIRST\_DOM}$ delay before transmitting the first dominant bit.
- Toggling the WAKE pin: Just before entering the Sleep mode, the WAKE pin state is stored. A change in the level longer than the deglitcher time (70 µs maximum) will generate a wake-up, and the device enters into the Awake Transitional mode, with INH High and RXD pulled Low. The device goes into Normal mode when EN is switched from Low to High and stays High for a delay higher than $t_{LWUE}$. Once in Normal mode, the device has to wait $t_{FIRST\_DOM}$ delay before transmitting the first dominant bit.

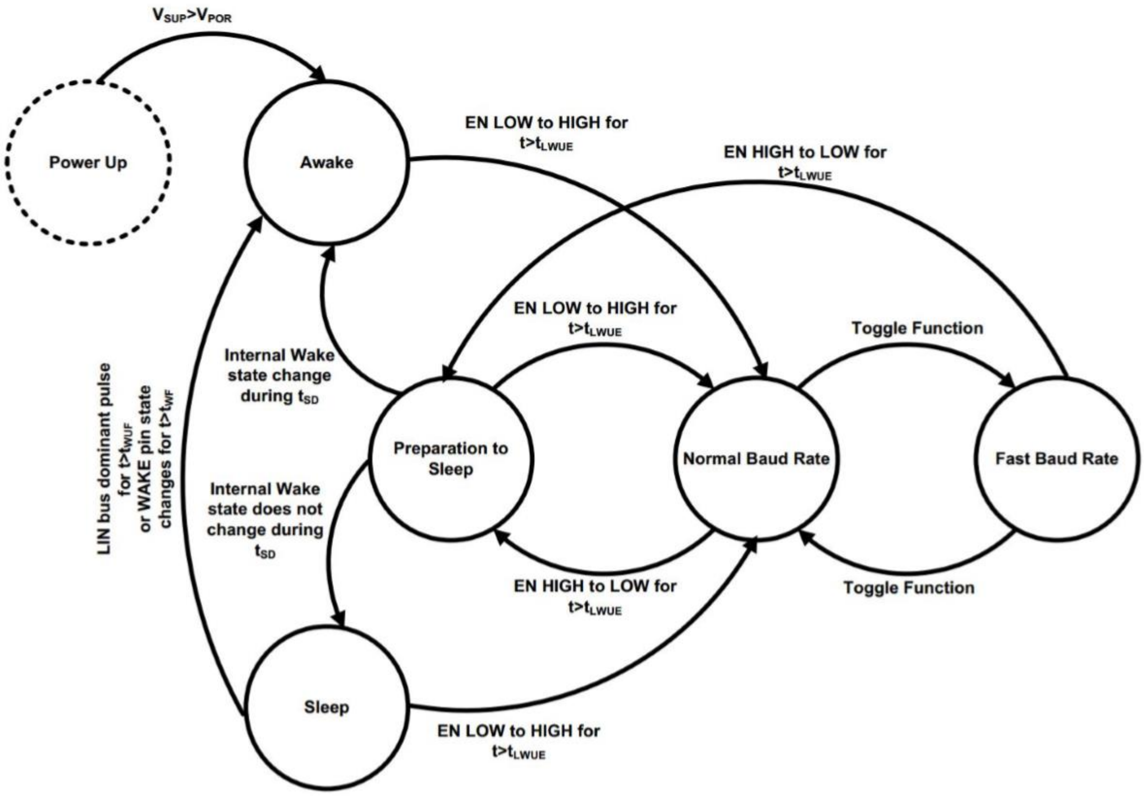



**Figure 12: Operational and transitional modes state diagram**

The following table explains Figure 12:

| Operational/ Transitional | LIN | INH | EN | TXD | RXD |
|---|---|---|---|---|---|
| Sleep | Recessive state, driver off with 725 kΩ pull-up | OFF (low) | LOW | X | High-impedance HIGH if external pull-up to VDD |
| Awake | Recessive state, driver off. 725 kΩ pull-up active | ON (high) | LOW | X | LOW. If external pull-up, HIGH-to-LOW transition reports wake-up |
| Preparation to Sleep mode | Recessive state, driver off with 725 kΩ pull-up | ON (high) | LOW | X | High-impedance. High if external pull-up to $V_{SUP}$ |
| Normal mode | Driver active. 30 kΩ pull-up active | ON (high) | HIGH | Low to drive LIN bus in dominant High to drive LIN bus in recessive | Report LIN bus state: • Low LIN bus dominant • High LIN bus recessive |

X = Don't care.

## 11.6 Fail Safe Features

The table below describes the device protections:

| Block | Fault | Functional mode | Condition | Response | Recovery condition | Recovery functionality mode |
|---|---|---|---|---|---|---|
| Power Supply | Power on Reset (POR) | All modes | $V_{SUP}$ < 3.5 V (min) then power up | No internal supplies | Condition gone | Device goes in Awake mode whatever the previous device mode |
| INH | INH Thermal Shutdown | Normal, Awake & Preparation to Sleep modes | Temperature > 160 °C (typical) | INH high side turned off. LIN transmitter and receiver in recessive state | Condition gone | Device returns in same functional mode |
| LIN | $V_{SUP}$ under-voltage | Normal | $V_{SUP}$ < $V_{UVL}$ | LIN transmitter in recessive state | Condition gone | Device returns in same functional mode |
| | TXD Pin Permanent Dominant | | TXD pin low for more than 5.0 ms (typical) | LIN transmitter in recessive state | Condition gone | Device returns in same functional mode |
| | LIN Thermal Shutdown | Normal | Temperature > 160 °C (typical) | LIN transmitter and receiver in recessive state INH high side turned off | Condition gone | Device returns in same functional mode |

# 12. Test Circuit for Transient Test Pulses and Their Limits

The following table shows the limits of test voltage for transient immunity tests:

| Test Pulse | $V_S$ (V) | Pulse repetition frequency (Hz) ($1/T_1$) | Test duration (min) | $R_i$(Ω) | Remarks |
|---|---|---|---|---|---|
| 1 | -100 | 2 | 1 for function test<br>10 for damage test | 10 | $t_2$ = 0 s |
| 2a | +75 | 2 | | 2 | |
| 3a | -150 | 10000 | | 50 | |
| 3b | +100 | 10000 | | 50 | |

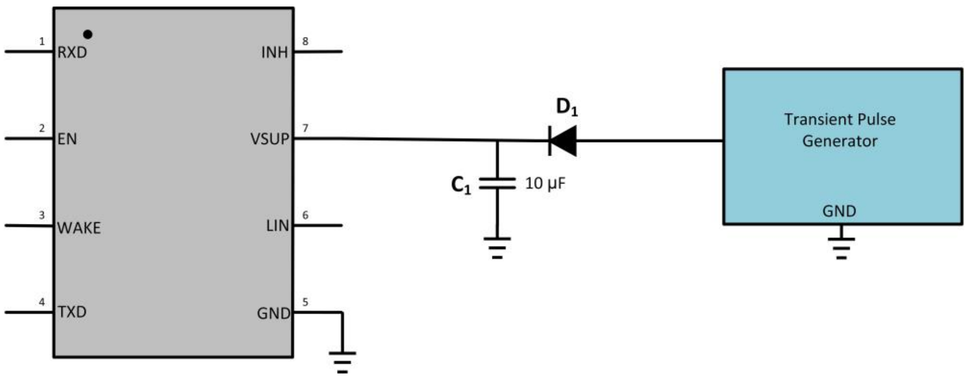



Figure 13: Test circuit for transient test pulses (VSUP)

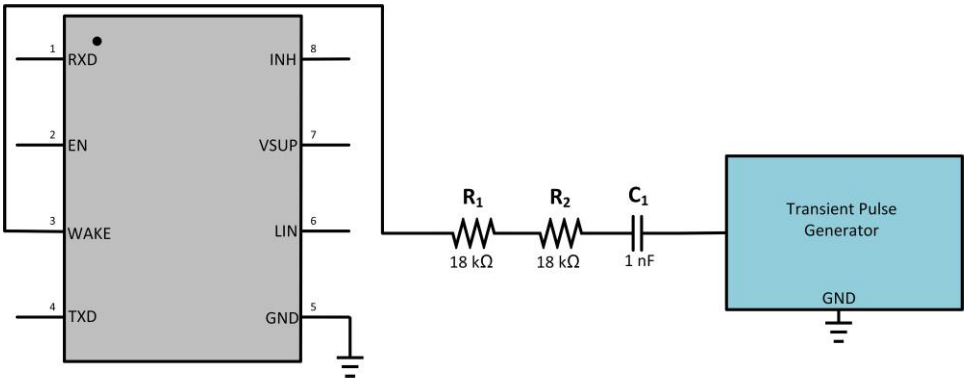



Figure 14: Test circuit for transient test pulses (WAKE)

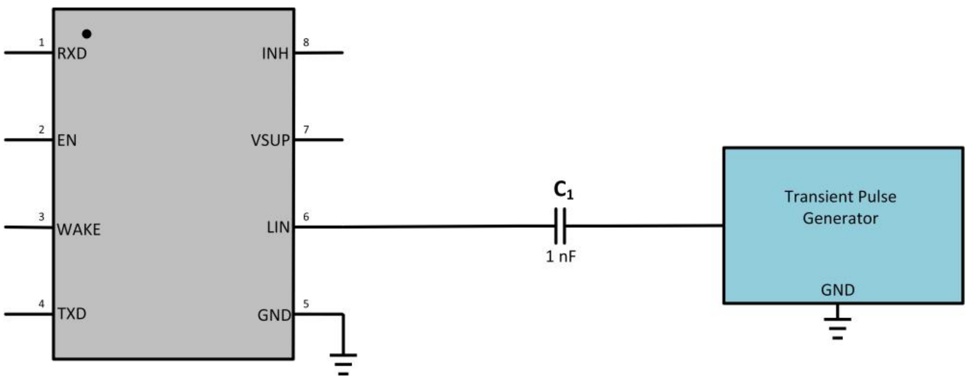



Figure 15: Test circuit for transient test pulses (LIN)

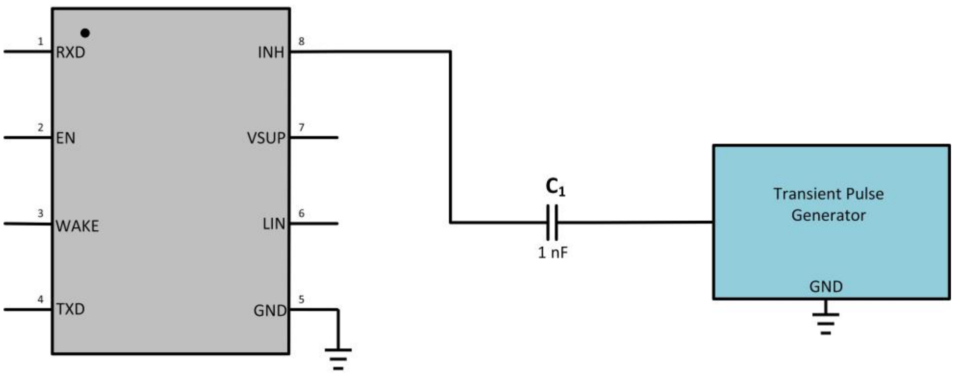
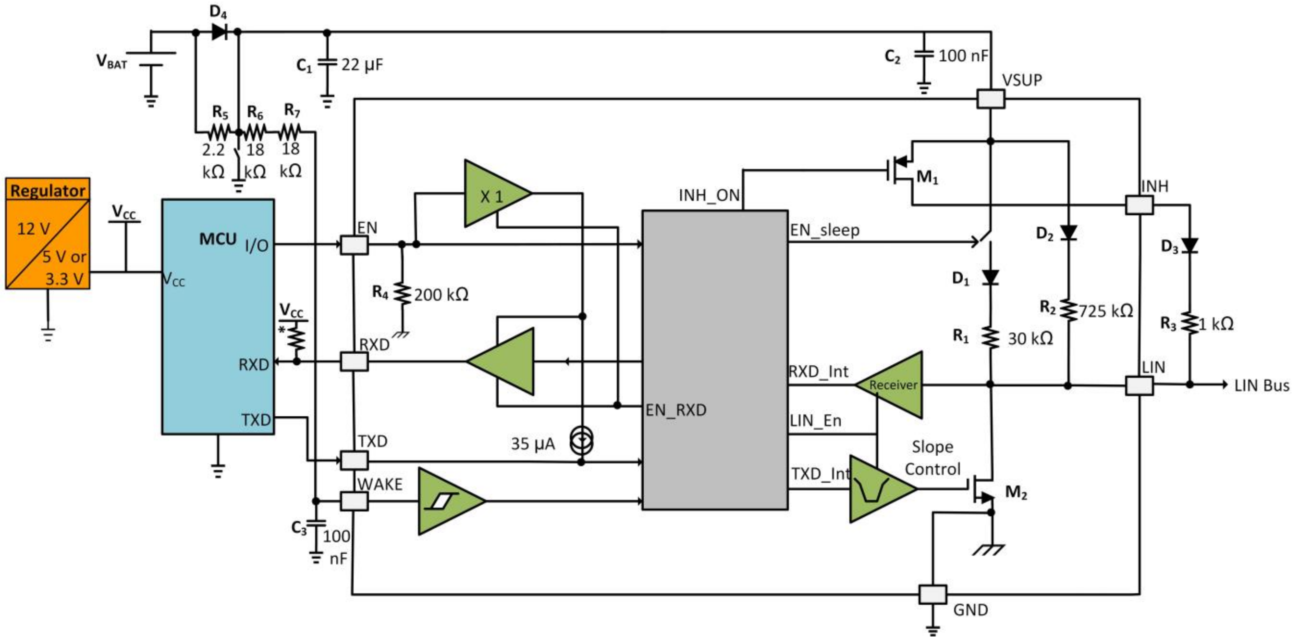



Figure 16: Test circuit for transient test pulses (INH)

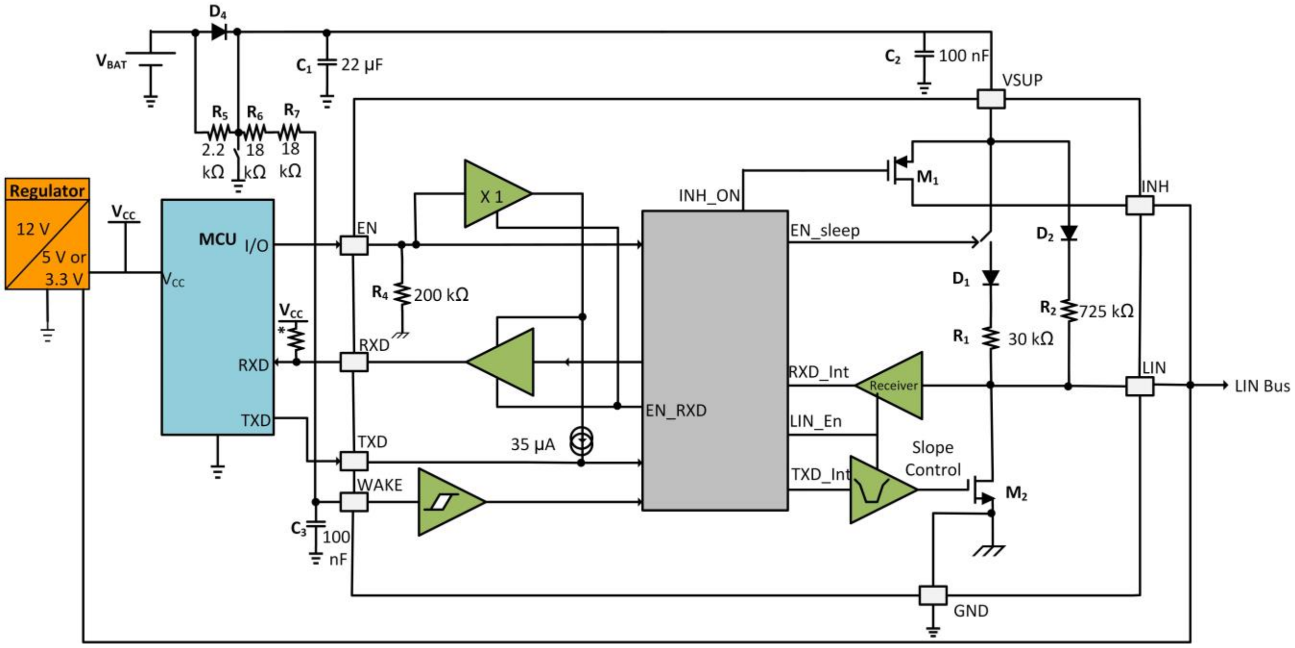
# 13. Applications

The device can be configured for several applications. Figure 17 and 18 show master and slave node applications. An additional pull-up resistor of 1.0 kΩ in series with a diode between the INH and LIN pins must be added when the device is used in the master node.




*: Optional. 2.2kΩ if implemented

Figure 17: Master node typical application




*: Optional. 2.2kΩ if implemented

Figure 18: Slave node typical application

# 14. Packaging

## 14.1 Summary

| | |
|---|---|
| **Terminal position code** | D (double) |
| **Package type descriptive code** | SO8 |
| **Package type industry code** | SO8 |
| **Package style descriptive code** | SO (small outline) |
| **Package body material type** | P (plastic) |
| **Mounting method type** | S (surface mount) |
| **Issue date** | 18-2-2003 |
| **Manufacturer package code** | SOT96 |

| Symbol | Parameter | Min | Nom | Max | Unit |
|---|---|---|---|---|---|
| A | Seated height | | 1.75 | 1.75 | mm |
| $A_2$ | Package height | 1.25 | 1.35 | 1.45 | mm |
| D | Package length | 4.8 | 4.9 | 5 | mm |
| e | Nominal pitch | | 1.27 | | mm |
| E | Package width | 3.8 | 3.9 | 4 | mm |
| $n_2$ | Actual quantity of termination | | 8 | | |

## 14.2 Package Outline

| Parameter | Min | Max | Unit |
|---|---|---|---|
| D[1] | 4.8 | 5 | mm |
| y | 0.1 | 0.1 | mm |

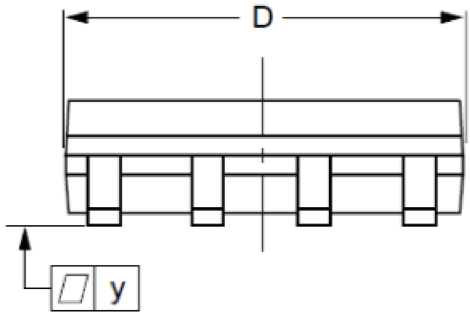



Figure 19

| Parameter | Min | Max | Unit |
|---|---|---|---|
| $A_{MAX}$ | 1.75 | 1.75 | mm |
| $A_1$ | 0.1 | 0.25 | mm |
| $A_2$ | 1.25 | 1.45 | mm |
| $A_3$ | 0.25 | 0.25 | mm |
| L | 1.05 | 1.05 | mm |
| $L_p$ | 0.4 | 1.0 | mm |
| Q | 0.6 | 0.7 | mm |
| θ | 0° | 8° | mm |

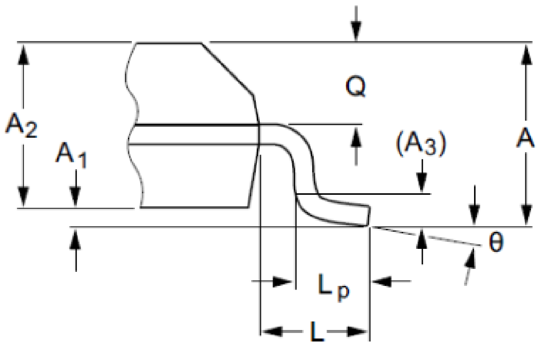



Figure 20

[1] Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| Parameter | Min | Max | Unit |
|---|---|---|---|
| c | 0.19 | 0.25 | mm |
| E[1] | 3.8 | 4.0 | mm |
| $H_E$ | 5.8 | 6.2 | mm |
| v | 0.25 | 0.25 | mm |

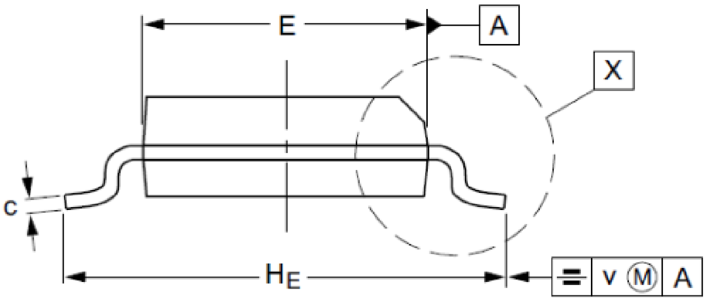



Figure 21

| Parameter | Min | Max | Unit |
|---|---|---|---|
| $b_p$ | 0.36 | 0.49 | mm |
| e | 1.27 | 1.27 | mm |
| w | 0.25 | 0.25 | mm |
| Z[2] | 0.3 | 0.7 | mm |

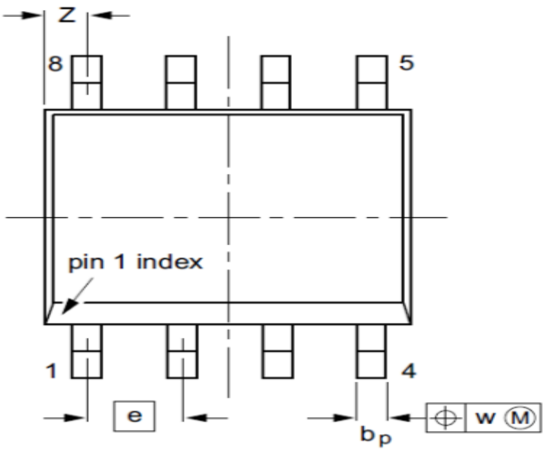



Figure 22

[1] Plastic or metal protrusions of 0.25 mm maximum per side are not included.
[2] Plastic or metal protrusions of 0.15 mm maximum per side are not included.

# Contents