

## 1. Introduction

The transceiver is designed for high-speed CAN applications in the automotive industry, providing the differential transmit and receive capability to (a microcontroller with) a CAN protocol controller. It offers improved Electro-Magnetic Compatibility (EMC) and Electro-Static Discharge (ESD) performance.

This CAN transceiver meets the ISO 11898-2:2003 and ISO 11898-5:2007 high speed CAN (Controller Area Network) physical layer standard. The transceiver has a low power standby mode with remote wake request feature. Additionally, includes protection feature to enhance device and network robustness.

## 2. Features

### 2.1 General

- SPLIT voltage output for stabilizing the recessive bus level
- Low Electro-Magnetic Emission (EME) and high Electro-Magnetic Immunity (EMI) based on IEC 62228 (2007)
- Suitable for 12 V and 24 V systems
- Timing guaranteed for data rates up to 5Mbit/s in the CAN FD fast phase
- Fully ISO 11898-2:2003 and ISO 11898-5:2007 compliant

### 2.2 Fail-safe behavior

- Low quiescent current in standby mode
- Remote wake-up pattern based on ISO11898-2 (2016)
- Under-voltage protection on  $V_{CC}$
- Functional behavior predictable under all supply conditions
- Transmit data (TXD) dominant time-out function
- Bus-dominant time-out function in standby-mode
- Transceiver disengages from the bus when not powered up (zero load)

### 2.3 Protections

- High ESD handling capability on the bus pins ( $\pm 8$  kV)
- Bus pins protected against transients in automotive environments
- Receiver common mode input voltage:  $\pm 40$  V
- Over temperature protection



### 3. Pinning information

Symbol	Description
TXD	Transmit data input
GND	Ground
V <sub>CC</sub>	Supply voltage
RXD	Receive data output; reads out data from the bus lines
SPLIT	Common-mode stabilization output
CANL	Low-level CAN bus line
CANH	High-level CAN bus line
STB	Standby mode control input

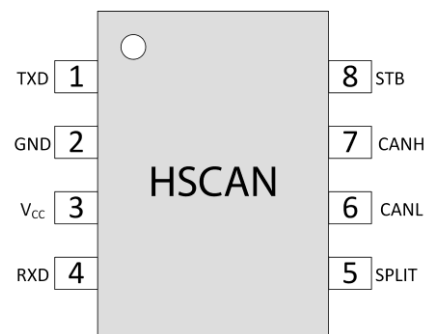


Figure 1: Pin configuration

### 4. Quick Reference

Symbol	Parameter	Condition	Min	typ	Max	Unit
V <sub>CANH</sub>	Voltage on pin CANH		-40		+40	V
V <sub>CANL</sub>	Voltage on pin CANL		-40		+40	V
V <sub>SPLIT</sub>	Voltage on pin SPLIT		-40		+40	V
V <sub>ESD</sub>	Electrostatic discharge voltage	IEC 61000-4-2 at pins CANH , CANL	-8		+8	KV
V <sub>CC</sub>	Supply voltage		4/5		5.5	V
I <sub>CC</sub>	Supply current	Standby mode	27.3	32.8	45.1	uA
		Normal mode : bus recessive	4.82	5.96	7.58	mA
		Normal mode : bus dominant	29.8	43.3	49.033	mA
T <sub>vj</sub>	Virtual junction temperature		-40		+150	°C
V <sub>TX,RX,STB</sub>	Logic voltage		-0.3		V <sub>CC</sub> + 0.3	V
V <sub>uvd</sub>	Undervoltage detection on pin V <sub>CC</sub>		1.3		2.7	V

### 5. Ordering information

Type number	Package		
	Name	Description	Version
QFN	SO <sub>8</sub>	plastic small outline package; 8 leads; body width 3.9 mm	0

## 6. Block Diagram

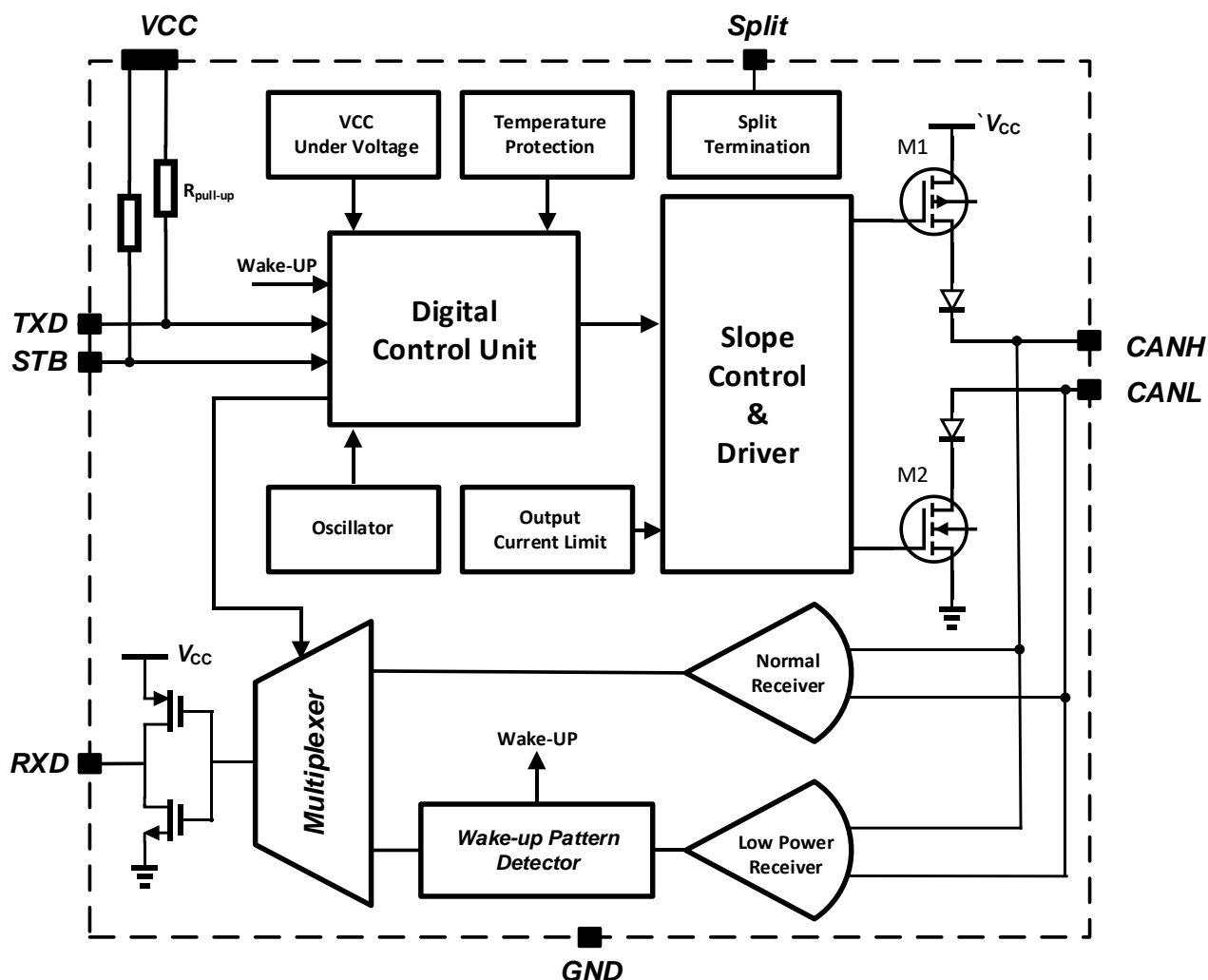


Figure 2: Block diagram

## 7. Functional Description

### 7.1 Operating mode

The transceiver supports two operating modes, Normal and Standby, which are selected via pin STB. See this table for a description of the operating modes under normal supply conditions.

Mode	Pin STB	Pin RXD	
		LOW	HIGH
Normal	LOW	Bus dominant	Bus recessive
Standby	HIGH	Wake-up request detected	No Wake-up request detected

### 7.1.1 Normal mode

A LOW level on pin STB selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines CANH and CANL (see [Figure 2](#) for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME.

### 7.1.2 Standby mode

A HIGH level on pin STB selects Standby mode. In Standby mode, the transceiver is not able to

transmit or correctly receive data via the bus lines. The transmitter and Normal-mode receiver blocks are switched off to reduce supply current, and only a low-power differential receiver monitors the bus lines for activity. The wake-up filter on the output of the low-power receiver does not latch bus dominant states, but ensures that only bus dominant and bus recessive states that persist longer than  $t_{\text{filtr(wake)bus}}$  are reflected on pin RXD.

In Standby mode, the bus lines are biased to ground to minimize the system supply current. When pin RXD goes LOW to signal a wake-up request, a transition to Normal mode will not be triggered until STB is forced LOW.

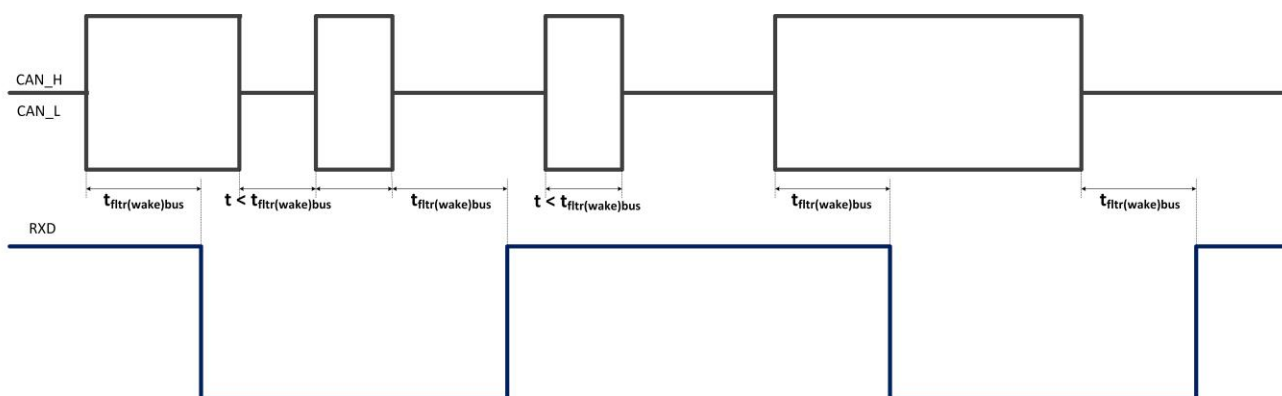


Figure 3 : Wake-up timing

## 7.2 Fail-Safe Features

### 7.2.1 TXD dominant time-out function

A 'TXD dominant time-out' timer is started when pin TXD is set LOW. If the LOW state on pin TXD persists for longer than  $t_{\text{to(dom)TXD}}$ , the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD is set to HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 40 Kbit/s.

### 7.2.2 Bus dominant time-out function

In Standby mode a 'bus dominant time-out' timer is started when the CAN bus changes from recessive to dominant state. If the dominant state on the bus persists for longer than  $t_{\text{to(dom)bus}}$ , the RXD pin is reset to HIGH. This function prevents a clamped dominant bus (due to a bus short-circuit or a failure in one of the other nodes on the network) from generating a permanent wake-up request. The bus dominant time-out timer is reset when the CAN bus changes from dominant to recessive state.

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### 7.2.3 Undervoltage detection

Should  $V_{CC}$  drop below the  $V_{CC}$  undervoltage detection level,  $V_{uvd(VCC)}$ , the transceiver will switch to Standby mode. The logic state of pin STB will be ignored until  $V_{CC}$  has recovered.

### 7.2.4 Overtemperature protection

The output drivers are protected against overtemperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature,  $T_{j(sd)}$ , the output drivers will be disabled until the virtual junction temperature falls below  $T_{j(sd)}$  and TXD becomes recessive again. Including the TXD condition ensures that output driver oscillation due to temperature drift is avoided.

### 7.3 Split pin

Using the SPLIT pin in conjunction with a split termination network (see [Figure 4](#) and [Figure 10](#)) can help to stabilize the recessive voltage level on the bus. This will reduce EME in networks with DC leakage to ground (e.g. from deactivated nodes with poor bus leakage performance). In Normal mode, pin SPLIT delivers a DC output voltage of  $0.5V_{CC}$ . In Standby mode or when  $V_{CC}$  is off, pin SPLIT is floating. When not used, the SPLIT pin should be left open.

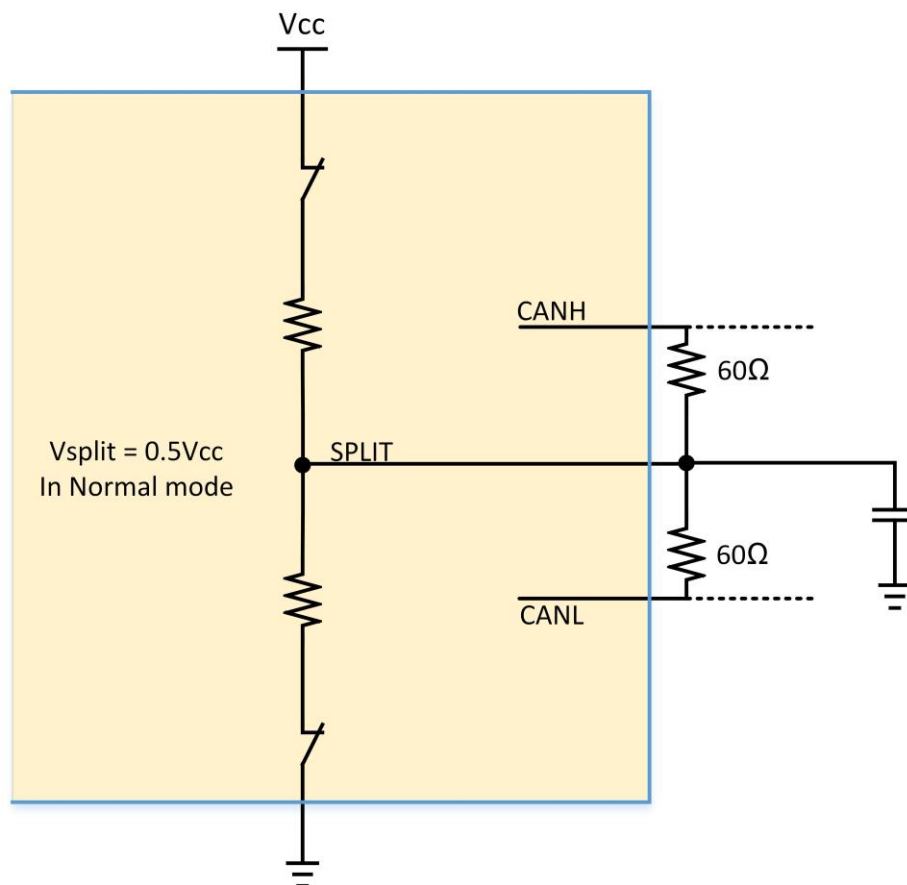


Figure 4 : Stabilization circuitry and application

## 8. Static characteristics

$T_{vj} = -40\text{ °C}$  to  $+150\text{ °C}$ ;  $V_{CC} = 4.5\text{ V}$  to  $5.5\text{ V}$ ;  $R_L = 60\ \Omega$  unless specified otherwise; All voltages are defined with respect to ground; Positive currents flow into the IC.<sup>[1]</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supply; pin V<sub>CC</sub></b>						
V <sub>CC</sub>	Supply voltage		4.5	-	5.5	V
V <sub>uvd(V<sub>CC</sub>)</sub>	Undervoltage detection voltage on pin V <sub>CC</sub>		3.8	-	4.12	V
I <sub>CC</sub>	Supply current	Standby mode	27.3	32.8	45.1	
		V <sub>TXD</sub> = V <sub>CC</sub>	-	10	15	μA
		Normal mode				
		Recessive; V <sub>TXD</sub> = V <sub>CC</sub>	4.82	6	7.58	mA
		Dominant; V <sub>TXD</sub> = 0V	30	43	49	mA
		Dominant; V <sub>TXD</sub> = 0V Short circuit on bus line 3 V < (V <sub>CANH</sub> = V <sub>CANL</sub> ) < +18 V	2.5	80	110	mA
<b>Standby mode control input; pin STB</b>						
V <sub>IH</sub>	High-level input voltage		0.7 V <sub>CC</sub>	-	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Low-level input voltage		-0.3	-	0.3 V <sub>CC</sub>	V
I <sub>IH</sub>	High-level input current	V <sub>STB</sub> = V <sub>CC</sub>	-1	-	1	μA
I <sub>IL</sub>	Low-level input current	V <sub>STB</sub> = 0 V	-15	-	-1	μA
<b>CAN transmit data input; pin TXD</b>						
V <sub>IH</sub>	High-level input voltage		0.7 V <sub>CC</sub>	-	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Low-level input voltage		-0.3	-	0.3 V <sub>CC</sub>	V
I <sub>IH</sub>	High-level input current	V <sub>STB</sub> = V <sub>CC</sub>	-5	-	+5	μA
I <sub>IL</sub>	Low-level input current	V <sub>TXD</sub> = 0 V	-260	-150	-30	μA
C <sub>i</sub> <sup>[2]</sup>	Input capacitance		-	5	10	pF
<b>CAN receive data output; pin RXD</b>						
I <sub>OH</sub>	High-level output current	V <sub>RXD</sub> = V <sub>CC</sub> + 0.4 V	-8	-3	-1	mA
I <sub>OL</sub>	Low-level output current	V <sub>RXD</sub> = 0.4 V; bus dominant	2	5	12	mA
<b>Bus lines; pins CANH and CANL</b>						
V <sub>O(dom)</sub>	Dominant output voltage	V <sub>TXD</sub> = 0 V; t < t <sub>to(dom)TXD</sub>				
		pin CANH; R <sub>L</sub> = 50 Ω to 65 Ω	2.75	3.5	4.5	V
		pin CANL; R <sub>L</sub> = 50 Ω to 65 Ω	0.5	1.5	2.25	V
V <sub>dom(TX)sym</sub>	Transmitter dominant voltage symmetry	V <sub>dom(TX)sym</sub> = V <sub>CC</sub> - V <sub>CANH</sub> - V <sub>CANL</sub>	-400	-	+400	mV
V <sub>TXsym</sub>	Transmitter voltage symmetry	V <sub>TXsym</sub> = V <sub>CANH</sub> + V <sub>CANL</sub> ; <sup>[2]</sup> f <sub>TXD</sub> = 250 kHz, 1 MHz and 2.5 MHz; C <sub>SPLIT</sub> = 4.7 nF; V <sub>CC</sub> = 4.5 V to 5.5 V <sup>[3]</sup>	0.89V <sub>CC</sub>	-	1.17V <sub>CC</sub>	V

<sup>[1]</sup> All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

<sup>[2]</sup> Calculated by design

<sup>[3]</sup> The test circuit used to measure the bus output voltage symmetry (which includes CSPLIT) is shown in [Figure 9](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{O(diff)}$	Differential output voltage	Dominant: Normal mode ; $V_{TXD} = 0\text{ V}$ ; $t < t_{to(dom)TXD}$ ; $V_{CC} = 4.75\text{ V to } 5.25\text{ V}$				
		$R_L = 45\Omega$	1.56	-	2.3	V
		$R_L = 75\Omega$	1.84	-	2.8	V
		$R_L = 2240\Omega$	4	-	4.8	V
		Recessive ; no load				
		Normal mode: $V_{TXD} = V_{CC}$ ; no load	-193	-	+3	mV
	Standby mode	0	-	0.5	mV	
$V_{O(rec)}$	Recessive output voltage	Normal mode; $V_{TXD} = V_{CC}$ ; no load	2	$0.5V_{CC}$	3	V
		Standby mode; no load	0.1		+0.1	V
$V_{th(RX)diff}$	Differential receiver threshold voltage	$-30\text{ V} \leq V_{CANL} \leq +30\text{ V}$ $-30\text{ V} \leq V_{CANH} \leq +30\text{ V}$				
		Normal mode	0.5	0.7	0.9	V
		Standby mode	0.4	0.7	1.15	V
$V_{rec(RX)}$	Receiver recessive voltage	Normal mode: $-12\text{ V} \leq V_{CANL} \leq +12\text{ V}$ $-12\text{ V} \leq V_{CANH} \leq +12\text{ V}$	-3	-	0.5	V
$V_{dom(RX)}$	Receiver dominant voltage	Normal mode; $-12\text{ V} \leq V_{CANL} \leq +12\text{ V}$ $-12\text{ V} \leq V_{CANH} \leq +12\text{ V}$	0.9	-	8.0	V
$V_{hys(RX)diff}$	Differential receiver hysteresis voltage	$-30\text{ V} \leq V_{CANL} \leq +30\text{ V}$ $-30\text{ V} \leq V_{CANH} \leq +30\text{ V}$	160	220	320	mV
$I_{O(sc)dom}$	Dominant short-circuit output current	$V_{TXD} = 0\text{ V}$ ; $t < t_{to(dom)TXD}$ ; $V_{CC} = 5\text{ V}$				
		pin CANH; $V_{CANH} = -3\text{V to } +40\text{V}$	-100	-70	-40	mA
		pin CANL; $V_{CANL} = -3\text{V to } +40\text{V}$	40	70	100	mA
$I_{O(sc)rec}$	Recessive short-circuit output current	Normal mode; $V_{TXD} = V_{CC}$ $V_{CANH} = V_{CANL} = -27\text{ to } 32\text{ V}$	-5	-	+5	mA
$I_L$	Leakage current	$V_{CC} = 0\text{ V}$ or $V_{CC} = \text{shorted to ground}$ via $47\text{ k}\Omega$ ; $V_{CANH} = V_{CANL} = 5\text{ V}$	-2.6	-	+2.6	$\mu\text{A}$
$R_i$	Input resistance		9	15	28	$\text{k}\Omega$
$R_i$	Input resistance deviation	Between $V_{CANH}$ and $V_{CANL}$	-1	-	+1	%
$R_{i(diff)}$	Differential input resistance		18	30	44.21	$\text{k}\Omega$
$C_{i(cm)}$ <sup>[1]</sup>	Common-mode input capacitance		-	-	20	pF
$C_{i(diff)}$ <sup>[1]</sup>	Differential input capacitance		-	-	10	pF
<b>Common mode stabilization output; pin SPLIT</b>						
$V_O$	Output voltage	Normal mode $I_{SPLIT} = -500\text{ }\mu\text{A to } +500\text{ }\mu\text{A}$	$0.34V_{CC}$	$0.5V_{CC}$	$0.65V_{CC}$	V
		Normal mode; $R_L = 1\text{ M}\Omega$	$0.45V_{CC}$	$0.5V_{CC}$	$0.5V_{CC}$	V
$I_L$	Leakage current	Standby mode $V_{SPLIT} = -40\text{ V to } +40\text{ V}$	0	-	19.5	$\mu\text{A}$
<b>Temperature detection</b>						
$T_{j(sd)}$ <sup>[1]</sup>	Shutdown junction temperature		-	190	-	$^{\circ}\text{C}$

<sup>1</sup> Calculated by design

## 9. Dynamic characteristic

$T_{vj} = -40\text{ }^{\circ}\text{C}$  to  $+150\text{ }^{\circ}\text{C}$ ;  $V_{CC} = 4.5\text{ V}$  to  $5.5\text{ V}$ ;  $R_L = 60\ \Omega$  unless specified otherwise; All voltages are defined with respect to ground; Positive currents flow into the IC.<sup>[1]</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Transceiver timing ; pins CANH, CANL, TXD and RXD; see <a href="#">figure 5</a> and <a href="#">figure 6</a></b>						
$t_{d(\text{TXD-busdom})}$	Delay time from TXD to bus dominant	Normal mode	-	65	-	ns
$t_{d(\text{TXD-busrec})}$	Delay time from TXD to bus recessive	Normal mode	-	90	-	ns
$t_{d(\text{busdom-RXD})}$	Delay time from bus dominant to RXD	Normal mode	-	60	-	ns
$t_{d(\text{busrec-RXD})}$	Delay time from bus recessive to RXD	Normal mode	-	65	-	ns
$t_{d(\text{TXDL-RXDL})}$	Delay time from TXD LOW to RXD LOW	Normal mode	60	-	220	ns
$t_{d(\text{TXDH-RXDH})}$	Delay time from TXD HIGH to RXD HIGH	Normal mode	60	-	220	ns
$t_{\text{bit}(\text{bus})}$	Transmitted recessive bit width	$t_{\text{bit}(\text{TXD})} = 500\text{ ns}$ <sup>[2]</sup>	435	-	530	ns
		$t_{\text{bit}(\text{TXD})} = 200\text{ ns}$ <sup>[2]</sup>	155	-	210	ns
$t_{\text{bit}(\text{RXD})}$	Bit time on pin RXD	$t_{\text{bit}(\text{TXD})} = 500\text{ ns}$ <sup>[2]</sup>	400	-	550	ns
		$t_{\text{bit}(\text{TXD})} = 200\text{ ns}$ <sup>[2]</sup>	120	-	220	ns
$\Delta t_{\text{rec}}$	Receiver timing symmetry	$t_{\text{bit}(\text{TXD})} = 500\text{ ns}$	-65	-	+40	ns
		$t_{\text{bit}(\text{TXD})} = 200\text{ ns}$	-45	-	+15	ns
$t_{\text{to}(\text{dom})\text{TXD}}$	TXD dominant time-out time	$V_{\text{TXD}} = 0\text{ V}$ ; Normal mode	0.3	2	5	ms
$t_{\text{to}(\text{dom})\text{bus}}$	Bus dominant time-out time	Standby mode	0.3	2	5	ms
$t_{\text{ftr}(\text{wake})\text{bus}}$	Bus wake-up filter time	Standby mode	3.2	3.5	4.14	$\mu\text{s}$
$t_{d(\text{stb-norm})}$	Standby to normal mode delay time		7	25	47	$\mu\text{s}$

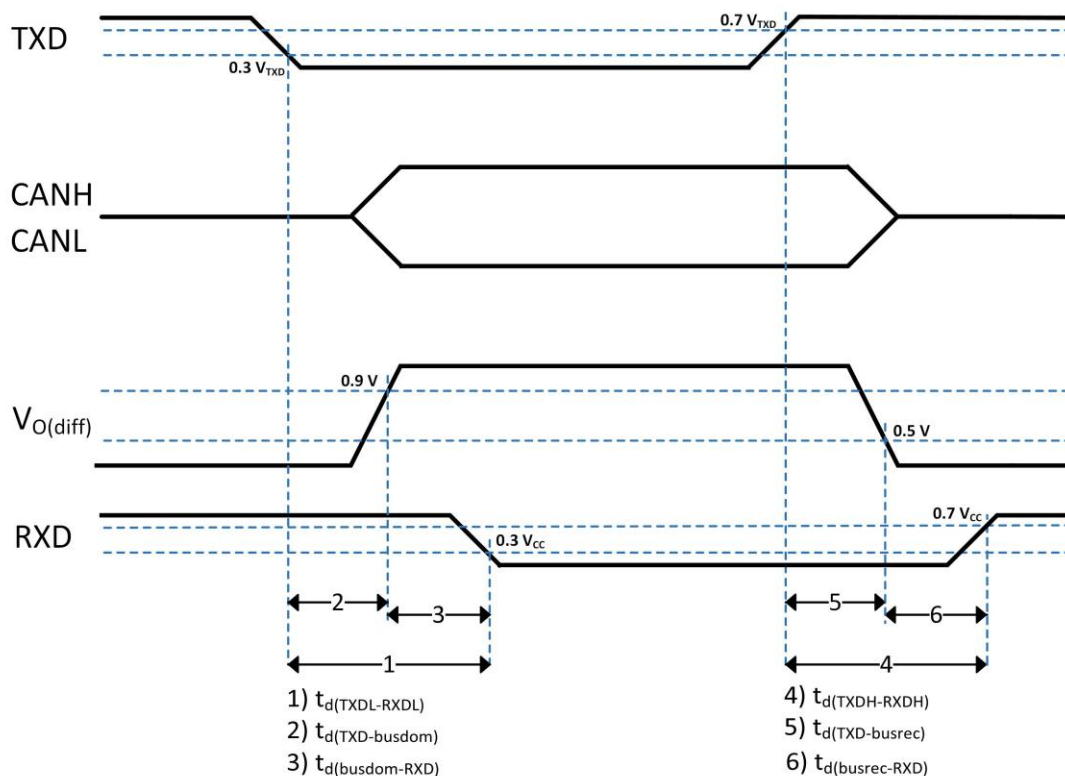


Figure 5 : Timing diagram

<sup>1</sup> All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

<sup>2</sup> See [figure 7](#)



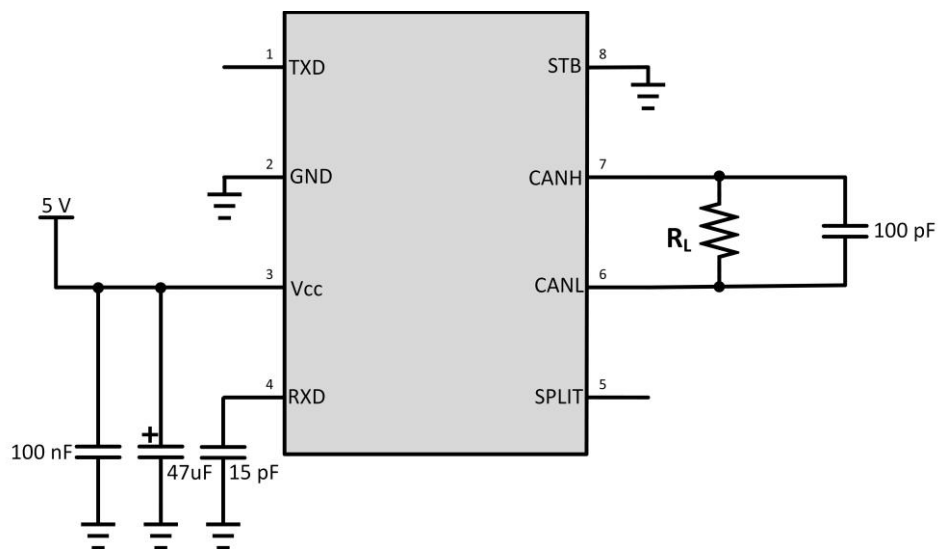
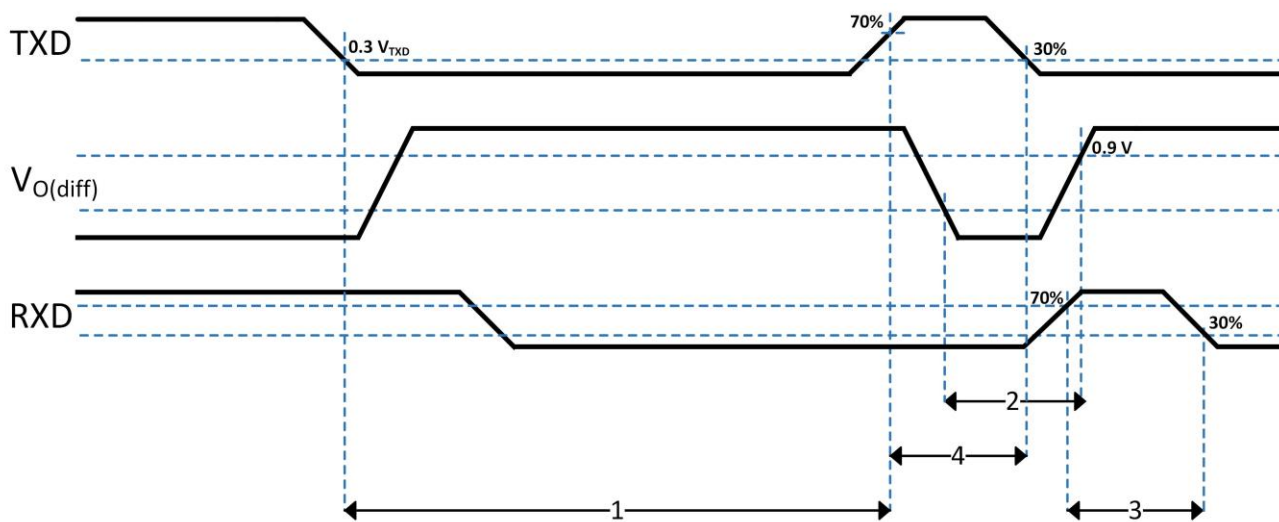


Figure 6 :Timing test circuit



- 1)  $5X t_{bit(TXD)}$
- 2)  $t_{bit(bus)}$
- 3)  $t_{bit(RXD)}$
- 4)  $t_{bit(TXD)}$

Figure 7 : Loop delay symmetry

## 10. Thermal characteristics

Symbol	Parameter	Condition	Value	Unit
$R_{th(vj-a)}$ <sup>[1]</sup>	thermal resistance from virtual junction to ambient	SO8 package; in free air	145	K/W

## 11. Absolute maximum ratings

Symbol	Parameter	Conditions	Min	Max	Unit
$V_x$	Voltage on pin x <sup>[2]</sup>	on pins CANH, CANL and SPLIT	-40	+40	V
$V_x$	Voltage on pin x	on pins TXD, RXD and STB	-0.3	$V_{CC} + 0.3$	V
$V_{diff}$	Differential voltage between pin CANH and pin CANL		-5	+10	V
$V_{trt}$	Transient voltage	on pins CANH, CANL <sup>[3]</sup>			
		pulse 1	-100	-	V
		pulse 2a	-	75	V
		pulse 3a	-150	-	V
		pulse 3b	-	100	V
$V_{ESD}$	Electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 $\Omega$ ) <sup>[4]</sup>			
		at pins CANH and CANL	-8	+8	kV
		Human Body Model (HBM); 100 pF, 1.5 k $\Omega$ <sup>[5]</sup>			
		at pins CANH and CANL	-8	+8	kV
		at any other pin	-4	+4	kV
		Machine Model (MM); 200 pF, 0.75 $\mu$ H, 10 $\Omega$ <sup>[6]</sup>			
		at any pin	-300	+300	V
		Charged Device Model (CDM); field Induced charge; 4 pF <sup>[7]</sup>			
at corner pins	-750	+750	V		
at any pin	-500	+500	V		
$T_{vj}$	Virtual junction temperature <sup>[8]</sup>		-40	+150	$^{\circ}$ C
$V_{CC}$	Supply voltage		-0.3	5.5	V

<sup>1</sup> According to IEC 60747-1

<sup>2</sup> The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.

<sup>3</sup> According to IEC TS 62228 (2007), Section 4.2.4; parameters for standard pulses defined in ISO7637 part 2: 2004-06.

<sup>4</sup> According to IEC TS 62228 (2007), Section 4.3; DIN EN 61000-4-2.

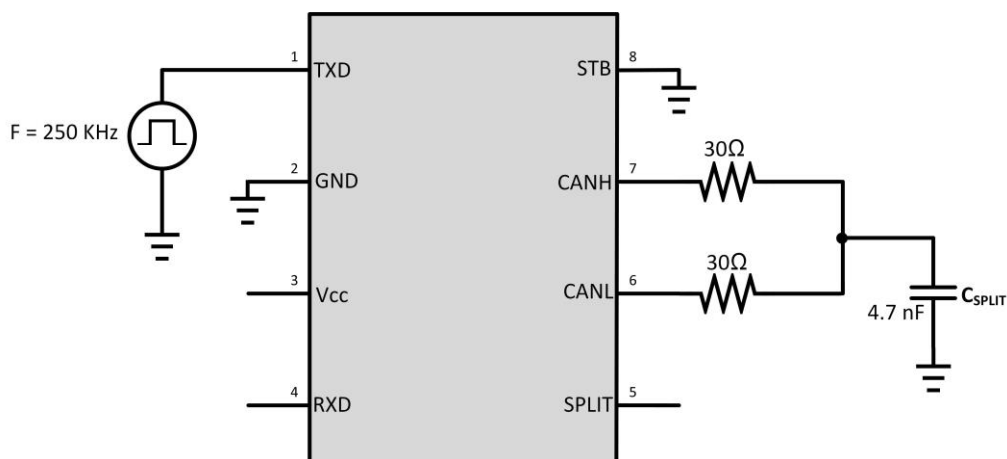
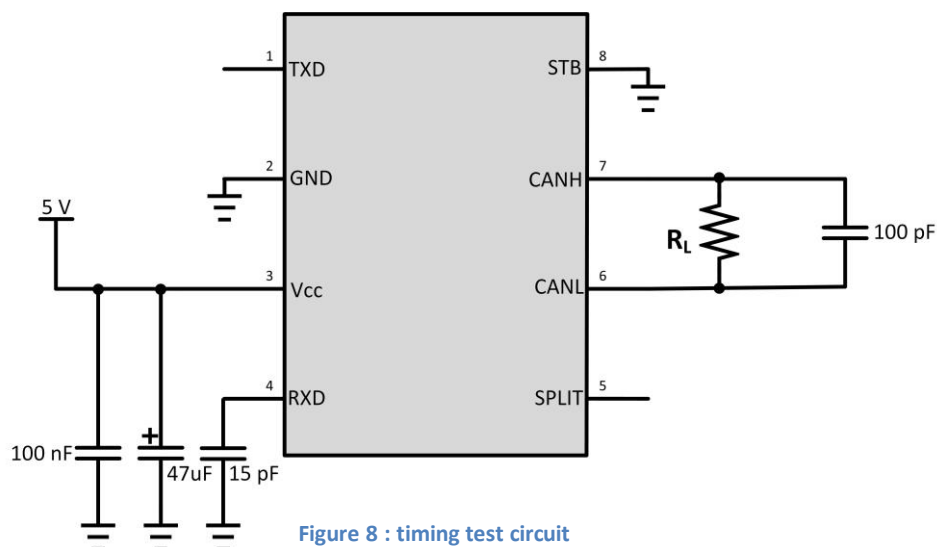
<sup>5</sup> According to AEC-Q100-002.

<sup>6</sup> According to AEC-Q100-003.

<sup>7</sup> According to AEC-Q100-011 Rev-C1. The classification level is C4B.

<sup>8</sup> In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is:  $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$  where  $R_{th(vj-a)}$  is a fixed value to be used for the calculation of  $T_{vj}$ . The rating for  $T_{vj}$  limits the allowable combinations of power dissipation (P) and ambient temperature ( $T_{amb}$ ).

## 12. Test information



### 12.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q100 Rev-G - Failure mechanism based stress test qualification for integrated circuits, and is suitable for use in automotive application.

## 13. Application information

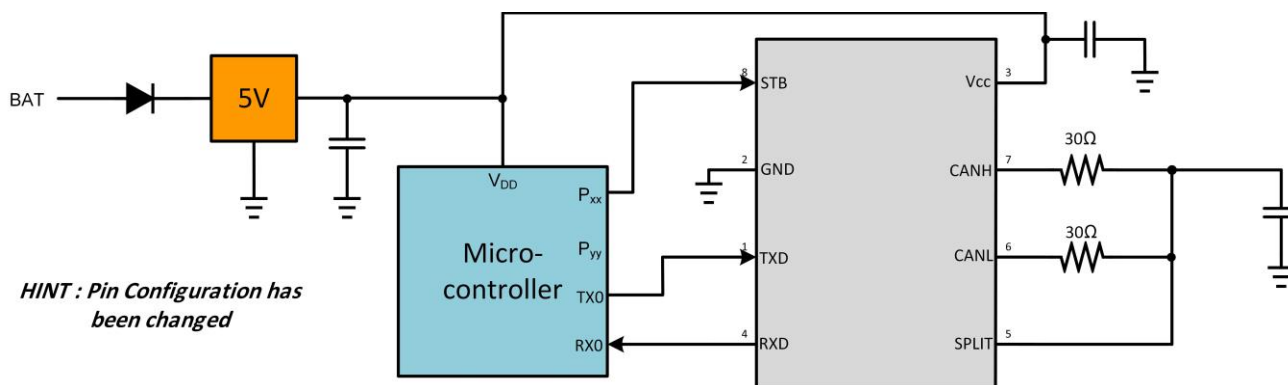


Figure 10 : Typical application with a 5V microcontroller

## 14. Packaging

### 14.1 Summary

Terminal position code	D (double)
Package type descriptive code	SO8
Package type industry code	SO8
Package style descriptive code	SO (small outline)
Package body material type	P (plastic)
Mounting method type	S (surface mount)
Issue date	18-2-2003
Manufacturer package code	SOT96

Symbol	Parameter	Min	Nom	Max	Unit
A	Seated height		1.75	1.75	mm
A <sub>2</sub>	Package height	1.25	1.35	1.45	mm
D	Package length	4.8	4.9	5	mm
e	Nominal pitch		1.27		mm
E	Package width	3.8	3.9	4	mm
n <sub>2</sub>	Actual quantity of termination		8		

## 14.2 Package outline

Parameter	Min	Max	Unit
D <sup>[*]</sup>	4.8	5	mm
y	0.1	0.1	mm

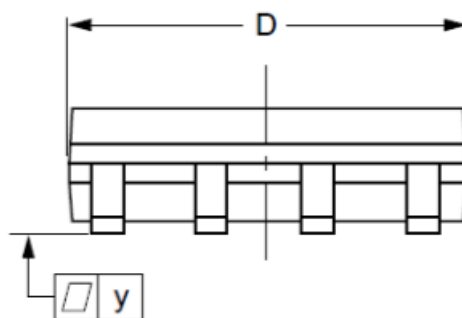


Figure 11

Parameter	Min	Max	Unit
A <sub>MAX</sub>	1.75	1.75	mm
A <sub>1</sub>	0.1	0.25	mm
A <sub>2</sub>	1.25	1.45	mm
A <sub>3</sub>	0.25	0.25	mm
L	1.05	1.05	mm
L <sub>p</sub>	0.4	1.0	mm
Q	0.6	0.7	mm
θ	0°	8°	mm

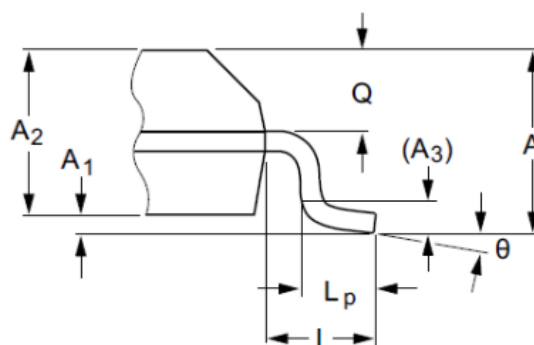


Figure 12

Parameter	Min	Max	Unit
c	0.19	0.25	mm
E <sup>[†]</sup>	3.8	4.0	mm
H <sub>E</sub>	5.8	6.2	mm
v	0.25	0.25	mm

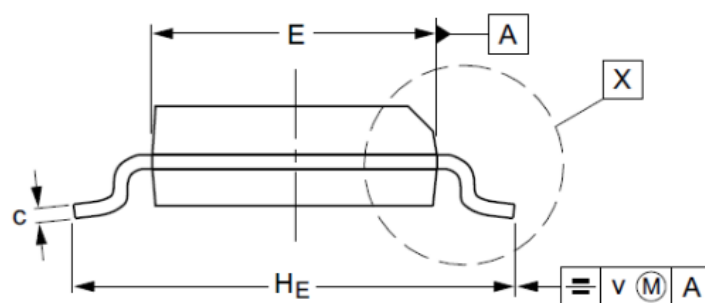


Figure 13

Parameter	Min	Max	Unit
b <sub>p</sub>	0.36	0.49	mm
e	1.27	1.27	mm
w	0.25	0.25	mm
Z <sup>[*]</sup>	0.3	0.7	mm

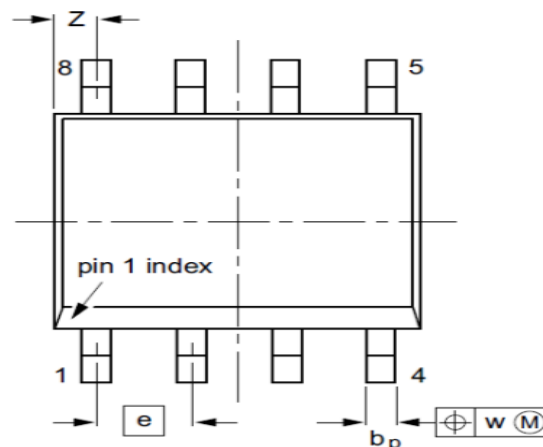


Figure 14

\* Plastic or metal protrusions of 0.15 mm maximum per side are not included

† Plastic or metal protrusions of 0.25 mm maximum per side are not included

## 15. Appendix : ISO 11898-2:2016 parameter

ISO 11898-2:2016		data sheet	
Parameter	Notation	Symbol	Parameter
<b>HS-PMA recessive output characteristics, bus biasing active/inactive</b>			
Single ended output voltage on CAN_H	$V_{CAN\_H}$	$V_{O(rec)}$	Recessive output voltage
Single ended output voltage on CAN_L	$V_{CAN\_L}$		
Differential output voltage	$V_{Diff}$	$V_{O(diff)}$	Differential output voltage
<b>Optional HS-PMA transmit dominant timeout</b>			
Transmit dominant timeout, long	$t_{dom}$	$t_{to(dom)TXD}$	TXD dominant time-out time
Transmit dominant timeout, short			
<b>HS-PMA dominant output characteristics</b>			
Single ended voltage on CAN_H	$V_{CAN\_H}$	$V_{O(dom)}$	Dominant output voltage
Single ended voltage on CAN_L	$V_{CAN\_L}$		
Differential voltage on normal bus load	$V_{Diff}$	$V_{O(diff)}$	Differential output voltage
Differential voltage on effective resistance during arbitration			
Optional: Differential voltage on extended bus load range			
<b>HS-PMA driver symmetry</b>			
Driver symmetry	$V_{SYM}$	$V_{TXsym}$	Transmitter voltage symmetry
<b>Maximum HS-PMA driver output current</b>			
Absolute current on CAN_H	$I_{CAN\_H}$	$I_{O(sc)dom}$	Dominant short-circuit output current
Absolute current on CAN_L	$I_{CAN\_L}$		
<b>HS-PMA static receiver input characteristics, bus biasing active/inactive</b>			
Recessive state differential input voltage range Dominant state differential input voltage range	$V_{Diff}$	$V_{th(RX)dif}$	Differential receiver threshold voltage
		$V_{rec(RX)}$	Receiver recessive voltage
		$V_{dom(RX)}$	Receiver dominant voltage
<b>HS-PMA implementation loop delay requirement</b>			
Loop delay	$t_{Loop}$	$t_{d(TXDH-RXDH)}$	Delay time from TXD HIGH to RXD HIGH
		$t_{d(TXDL-RXDL)}$	Delay time from TXD LOW to RXD LOW
<b>HS-PMA receiver input resistance (matching)</b>			
Differential internal resistance	$R_{Diff}$	$R_{i(dif)}$	Differential input resistance
Single ended internal resistance	$R_{CAN\_H}$ $R_{CAN\_L}$	$R_i$	Input resistance
Matching of internal resistance	MR	$\Delta R_i$	Input resistance deviation
<b>Optional HS-PMA implementation data signal timing requirements for use with bit rates above 1 Mbit/s up to 2 Mbit/s and above 2 Mbit/s up to 5 Mbit/s</b>			
Transmitted recessive bit width @ 2 Mbit/s / @ 5 Mbit/s, intended	$t_{Bit(Bus)}$	$t_{bit(bus)}$	Transmitted recessive bit width
Received recessive bit width @ 2 Mbit/s / @ 5 Mbit/s	$t_{Bit(RXD)}$	$t_{bit(RXD)}$	Bit time on pin RXD
Receiver timing symmetry @ 2 Mbit/s / @ 5 Mbit/s	$\Delta t_{Rec}$	$\Delta t_{rec}$	Receiver timing symmetry
<b>HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered</b>			
Leakage current on CAN_H, CAN_L	$I_{CAN\_H}$ $I_{CAN\_L}$	$I_L$	Leakage current

ISO 11898-2:2016		data sheet	
Parameter	Notation	Symbol	Parameter
<b>HS-PMA maximum ratings of <math>V_{CAN\_H}</math>, <math>V_{CAN\_L}</math> and <math>V_{Diff}</math></b>			
Maximum rating $V_{Diff}$	$V_{Diff}$	$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL
General maximum rating $V_{CAN\_H}$ and $V_{CAN\_L}$	$V_{CAN\_H}$	$V_x$	voltage on pin x
Optional: Extended maximum rating $V_{CAN\_H}$ and $V_{CAN\_L}$	$V_{CAN\_L}$		
<b>HS-PMA bus biasing control timings</b>			
CAN activity filter time, long	$t_{Filter}$	$t_{wake(bus-dom)}^{*†}$	bus dominant wake-up time
CAN activity filter time, short		$t_{wake(bus-rec)}$	bus recessive wake-up time
Wake-up timeout, short	$t_{Wake}$	$t_{to(wake)bus}$	bus wake-up time-out time
Wake-up timeout, long			
Timeout for bus inactivity	$t_{Silence}$	$t_{to(silence)}$	bus silence time-out time
Bus Bias reaction time	$t_{Bias}$	$t_{d(busact-bias)}$	delay time from bus active to bias

\*  $t_{fitr(wake)bus}$  - bus wake-up filter time, in devices with basic wake-up functionality

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